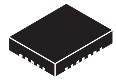
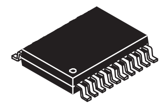


RHF 24-Pin



PWP 20-Pin

DUAL-PORT, LOW-POWER DIFFERENTIAL xDSL LINE DRIVER AMPLIFIERS

FEATURES

- **Trimmed Low-Power Consumption**
  - **4.2-mA/amp Full Bias Mode; 4.8 mA Max**
  - **3.2-mA/amp Mid Bias Mode; 3.7 mA Max**
  - **2.15-mA/amp Low Bias Mode; 2.5 mA Max**
  - **Shutdown Mode and I_{ADJ} Pin for Variable Bias**
- **Low Noise**
  - **3-nV/√Hz Voltage Noise**
  - **5.9-pA/√Hz Inverting Current Noise**
  - **1.2-pA/√Hz Noninverting Current Noise**
- **Low MTPR Distortion**
  - **–74 dB with ADSL and ADSL2**
  - **–71 dB with ADSL2+ and –70 dB with ADSL2++**
- **–83 dBc THD (1 MHz, 100-Ω Differential)**
- **High Output Current: >415 mA (25-Ω Load)**
- **Wide Output Swing: 44 Vpp (±12-V, 200-Ω Differential)**
- **Wide Bandwidth: 30 MHz (Gain = 5)**
- **Wide Power Supply Range: ±4 V to ±16 V**

APPLICATIONS

- **Ideal For Power Sensitive, High Density ADSL, ADSL2, ADSL2+, and ADSL2++ Systems**

DESCRIPTION

The THS6184 is a dual-port, low-power current feedback differential line driver amplifier system ideal for xDSL systems. Its extremely low-power dissipation is ideal for ADSL, ADSL2, ADSL2+, and ADSL2++ systems that must achieve high densities in ADSL central office applications by combining two ports, or four amplifiers, into one package.

The unique architecture of the THS6184 allows the trimmed quiescent current to be much lower than existing line drivers while still achieving high linearity. Distortion at these low-power levels is good with –83-dBc THD at 1 MHz with the low bias mode of 4.2 mA/port. Fixed and variable multiple-bias settings of the amplifiers allows for enhanced power savings for line lengths where the full performance of the amplifier is not required.

The wide output swing of 44-Vpp differentially with ±12-V power supplies coupled with over 415-mA current drive allow for wide dynamic range, keeping distortion minimized. With a low 3-nV/√Hz voltage noise coupled with a low 5.9-pA/√Hz inverting current noise, the THS6184 increases the sensitivity of the receive signals allowing for better margins and reach.

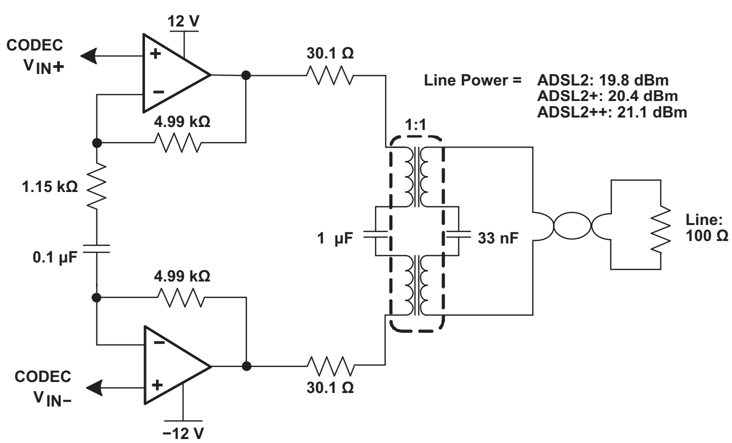


Figure 1. Typical Line Driver Circuit Using One Port of THS6184

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)[1]

			UNIT
V_{S-} to V_{S+}	Supply voltage		33 V
V_I	Input voltage		$\pm V_S$
V_{ID}	Differential input voltage		±2 V
I_O	Output current – Static DC[2]		±100 mA
	Continuous power dissipation		See Dissipation Rating Table
T_J	Maximum junction temperature, any condition[3]		150°C
	Maximum junction temperature, continuous operation, long term reliability[4]		130°C
Tstg	Storage temperature range		–65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300°C
	ESD ratings	HBM	900 V
		CDM	1500 V
		MM	100 V

(1) Stresses above those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied Exposure to absolute maximum rated conditions for extended periods may degrade device reliability.
(2) The THS6184 incorporates a PowerPAD™ on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI Technical Brief SLMA002 for more information about utilizing the PowerPAD™ thermally enhanced package. Under high frequency ac operation (>10 kHz), the short-term output current capability is much greater than the continuous DC output current rating. This short-term output current rating is about 8.5X the dc capability, or about ±850 mA.
(3) The absolute maximum junction temperature under any condition is limited by the constraints of the silicon process.
(4) The absolute maximum junction temperature for continuous operation is limited by the package constraints. Continuous operation above this temperature may result in reduced reliability and/or lifetime of the device.

DISSIPATION RATINGS

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)[1]	POWER RATING[2] T_J = 130°C	
			T_A = 25°C	T_A = 85°C
QFN-24 (RHF)	1.7	32[3]	3.3 W	1.4 W
HTSSOP-20 (PWP)	27.5	45	2.3 W	1 W

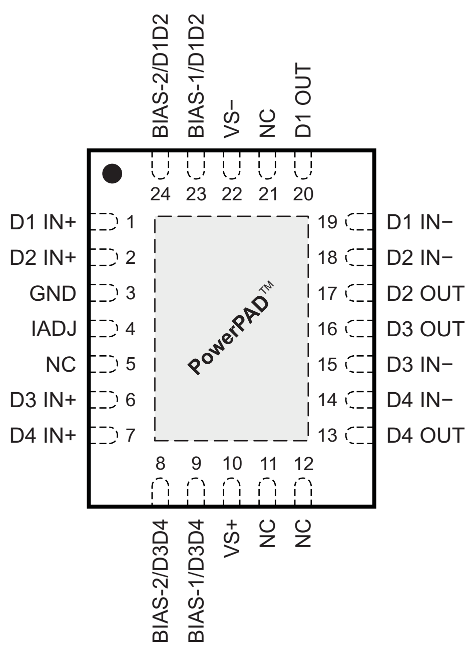
(1) This data was taken using a 4-layer, 3-inch × 3-inch test PCB with the PowerPAD soldered to the PCB. For high power dissipation applications, soldering the PowerPAD to the PCB is required. Failure to do so may result in reduced reliability and/or lifetime of the device. See TI technical brief SLMA002 for more information about utilizing the PowerPAD thermally enhanced package.
(2) Power rating is determined with a junction temperature of 130°C. This is the point where distortion starts to substantially increase and long-term reliability starts to be reduced. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance and reliability.
(3) If the PowerPAD is not soldered to the PCB, the θ_{JA} increases to 74°C/W for the RHF package.

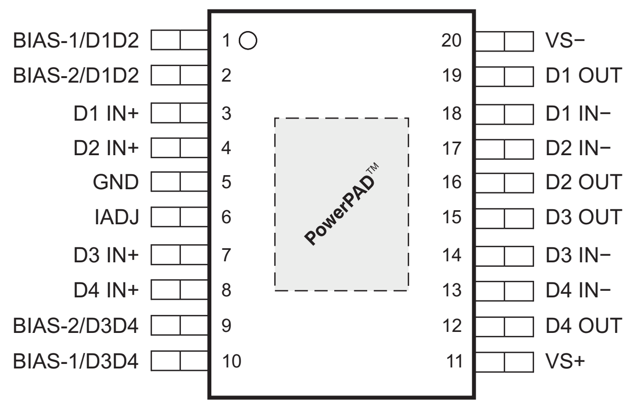
PACKAGING/ORDERING INFORMATION(1)

PACKAGED DEVICES(2)	DEVICE MARKING	PACKAGE TYPE	TRANSPORT MEDIA, QUANTITY
THS6184RHFT	6184	QFN-24	Tape and reel, 250
THS6184RHFR			Tape and reel, 3000
THS6184PWP	THS6184	PowerPAD™ HTSSOP-20	Rails, 70
THS6184PWPR			Tape and reel, 2000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) The thermal pad is electrically isolated from all other pins.

PIN CONFIGURATION





See Notes

NC − No internal connection
See Notes

A. The THS6184 defaults to the FULL BIAS state if no signal is present on the BIAS pins.
B. The PowerPAD is electrically isolated from all other pins and can be connected to any potential voltage range from V_{S-} to V_{S+}. Typically, the PowerPAD is connected to the GND plane as this plane tends to be physically the largest and able to dissipate the most amount of heat.
C. The GND pin range is from V_{S-} to (V_{S+} – 2.5 V).
D. The I_{ADJ} (RHF pin 4, PWP pin 6) must be connected to GND (RHF pin 3, PWP pin 5) for full bias as used in the specification tables.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{S-} to V_{S+}	Supply voltage	Dual supply	±4	±16	V
		Single supply	8	32	
T_A	Operating free-air temperature		–40	85	°C
T_J	Operating junction temperature, continuous operating temperature		–40	130	

ELECTRICAL CHARACTERISTICS

V_S = ±12 V: R_F = 3 kΩ, R_L = 50 Ω, G = +5, R_{adj} = 0 Ω, full bias (unless otherwise noted) each amplifier independently tested

PARAMETER	CONDITIONS	TYP 25°C	OVER TEMPERATURE 25°C	0°C to 70°C	–40°C to 85°C	UNITS	MIN/MAX
AC PERFORMANCE							
Small-signal bandwidth, – 3 dB (V_O = 100 mV_{rms})	G = +1, R_F = 4 kΩ	50				MHz	Typ
Small-signal bandwidth, – 3 dB (V_O = 100 mV_{rms})	G = +2, R_F = 3.5 kΩ	40				MHz	Typ
Small-signal bandwidth, – 3 dB (V_O = 100 mV_{rms})	G = +5, R_F = 3 kΩ	30				MHz	Typ
Small-signal bandwidth, – 3 dB (V_O = 100 mV_{rms})	G = +10, R_F = 3 kΩ	22				MHz	Typ
0.1-dB bandwidth flatness	G = +5	8				MHz	Typ
Large-signal bandwidth	G = +5, V_O = 10 Vpp	17.5				MHz	Typ
Slew rate (25% to 75% level)	G = +5, V_O = 16-V step, single-ended	340				V/µs	Typ
Slew rate (25% to 75% level)	G = +5, V_O = 16-V Step, Differential	560				V/µs	Typ
Rise and fall time	G = +5, V_O = 2-Vpp	12				ns	Typ
Harmonic distortion, 2nd harmonic	G = +5, V_O = 2 Vpp, f = 1 MHz, Differential, R_L = 100 Ω	–89				dBc	Typ
Harmonic distortion, 2nd harmonic	G = +5, V_O = 2 Vpp, f = 1 MHz, Differential, R_L = 50 Ω	–85				dBc	Typ
Harmonic distortion, 3rd harmonic	G = +5, V_O = 2 Vpp, f = 1 MHz, Differential, R_L = 100 Ω	–85				dBc	Typ
Harmonic distortion, 3rd harmonic	G = +5, V_O = 2 Vpp, f = 1 MHz, Differential, R_L = 50 Ω	–79				dBc	Typ
Harmonic distortion, 2nd harmonic	G = +5, V_O = 2 Vpp, f = 4 MHz, Differential, R_L = 100 Ω	–83				dBc	Typ
Harmonic distortion, 2nd harmonic	G = +5, V_O = 2 Vpp, f = 4 MHz, Differential, R_L = 50 Ω	–80				dBc	Typ
Harmonic distortion, 3rd harmonic	G = +5, V_O = 2 Vpp, f = 4 MHz, Differential, R_L = 100 Ω	–63				dBc	Typ
Harmonic distortion, 3rd harmonic	G = +5, V_O = 2 Vpp, f = 4 MHz, Differential, R_L = 50 Ω	–55				dBc	Typ
Multitone Power Ratio (MTPR) 160 kHz to ADSL limit(1)	G = +10, PLine = +19.8 dBm, ADSL2	–74				dBc	Typ
Multitone Power Ratio (MTPR) 160 kHz to ADSL limit(1)	G = +10, PLine = +20.4 dBm, ADSL2+	–71				dBc	Typ
Multitone Power Ratio (MTPR) 160 kHz to ADSL limit(1)	G = +10, PLine = +21.1 dBm, ADSL2++	–70				dBc	Typ
Receive Band Spill-Over 25kHz to 138 kHz	G = +10, PLine = +19.8 dBm, ADSL2	–93				dBc	Typ
Receive Band Spill-Over 25kHz to 138 kHz	G = +10, PLine = +20.4 dBm, ADSL2+	–91				dBc	Typ
Receive Band Spill-Over 25kHz to 138 kHz	G = +10, PLine = +21.1 dBm, ADSL2++	–90				dBc	Typ
Input voltage noise	f > 10 kHz	3.0				nV/√Hz	Typ
Inverting current noise	f > 10 kHz	5.9				pA/√Hz	Typ
Noninverting current noise	f > 10 kHz	1.2				pA/√Hz	Typ
DC PERFORMANCE							
Open-loop transimpedance gain	R_L = 100 Ω	6				MΩ	Typ
Input offset voltage		±10	±22	±25	±25	mV	Max
Average offset voltage drift		±7				µV/°C	Typ
Input offset voltage matching	Channels 1 to 2 and 3 to 4 only	±0.5	±3	±5	±5	mV	Max
Noninverting Input bias current		±1	±10	±15	±15	µA	Max
Noninverting input bias current drift		±150				nA/°C	Typ
Inverting input bias current		±1	±10	±15	±15	µA	Max
Inverting input bias current drift		±150				nA/°C	Typ
INPUT CHARACTERISTICS							
Common-mode input range	RHF package	±10.8	±10	±9.9	±9.9	V	Min
Common-mode input range	PWP package	±10.2	±9.5	±9.4	±9.4	V	Min
Common-mode rejection ratio		67	60	58	58	dB	Min
Noninverting input resistance		500‖2				kΩ‖pF	Typ
Inverting input resistance		160				Ω	Typ

(1) Test circuit is as shown in Figure 2. Transformer insertion loss = 0.4 dB. ADSL2++ is still considered a proposal and is not an official standard at this time.

ELECTRICAL CHARACTERISTICS (continued)

V_S = ±12 V: R_F = 3 kΩ, R_L = 50 Ω, G = +5, R_{adj} = 0 Ω, full bias (unless otherwise noted) each amplifier independently tested

PARAMETER	CONDITIONS		TYP	OVER TEMPERATURE				
			25°C	25°C	0°C to 70°C	–40°C to 85°C	UNITS	MIN/ MAX
OUTPUT CHARACTERISTICS								
Output voltage swing	R_L = 100 Ω		+11				V	Typ
			–11				V	Typ
	R_L = 50 Ω		+10.8	+10.4	+10.3	+10.3	V	Min
			–10.8	–10.4	–10.3	–10.3	V	Max
	R_L = 25 Ω		+10.4	+9.8	+9.7	+9.7	V	Min
			–10.35	–9.7	–9.6	–9.6	V	Max
Output current (sourcing)	R_L = 25 Ω		416	392	388	388	mA	Min
Output current (sinking)	R_L = 25 Ω		414	388	384	384	mA	Min
Short circuit output Current			±850				mA	Typ
Output impedance	f = 1 MHz		0.2				Ω	Typ
Crosstalk	f = 1 MHz, Vo = 2 Vpp	D1 to D2, D3 to D4	–40				dB	Typ
		D1 to D3, D2 to D4	–70				dB	Typ
POWER SUPPLY								
Maximum operating voltage				±16.0	±16.0	±16.0	V	Max
Minimum operating voltage				±4.0	±4.0	±4.0	V	Min
Maximum Is+ quiescent current	Per amplifier, Full (Bias-1=0, Bias-2 = 0)		4.3	4.9	5.1	5.2	mA	Max
	Per amplifier, Mid (Bias-1=1, Bias-2 = 0)		3.3	3.8	4.0	4.1		
	Per amplifier, Low (Bias-1=0, Bias-2 = 1)		2.2	2.6	2.8	2.9		
	Per amplifier, Off (Bias-1=1, Bias-2 = 1)		0.2	0.3	0.4	0.4		
Minimum Is+ quiescent current	Per amplifier, Full (Bias-1=0, Bias-2 = 0)		4.3	3.8	3.6	3.6	mA	Min
Maximum Is- quiescent current	Per amplifier, Full (Bias-1=0, Bias-2 = 0)		4.1	4.7	4.9	5.0	mA	Max
	Per amplifier, Mid (Bias-1=1, Bias-2 = 0)		3.1	3.6	3.8	3.9		
	Per amplifier, Low (Bias-1=0, Bias-2 = 1)		2.1	2.4	2.6	2.7		
	Per amplifier, Off (Bias-1=1, Bias-2 = 1)		0.01	0.1	0.15	0.15		
Minimum Is- quiescent current	Per amplifier, Full Bias		4.1	3.6	3.5	3.5	mA	Min
Current through GND pin	Per amplifier, Full (Bias-1 = 0, Bias-2 = 0)		0.2				mA	Typ
Power supply rejection (+PSRR)	V_{S+} = 13 V to 11 V, V_{S-} = –12 V		78	72	70	69	dB	Min
Power supply rejection (-PSRR)	V_{S+} = 12 V, V_{S-} = –13 V to –11 V		73	67	65	64	dB	Min
LOGIC CHARACTERISTICS								
Bias control pin logic threshold	Logic 1, with respect to GND pin (2)		≥2.6				V	Typ
	Logic 0, with respect to GND pin (2)		≤0.8				V	Typ
Bias pin quiescent current	Bias-X =0.5 V (Logic 0)		1	10	15	15	µA	Max
	Bias-X = 3.3 V (Logic 1)		10	20	30	30		
Turn on time delay($t_{(ON)}$)	Time for I_S to reach 50% of final value		1				µs	Typ
Turn off time delay ($t_{(Off)}$)			1					
Bias pin input impedance			50				kΩ	Typ
Amplifier output impedance	Off (Bias-1 = 1, Bias-2 = 1)		10‖5				kΩ‖pF	Typ

(2) GND pin useable range is from V_{S-} to (V_{S+} – 2.5 V).

Table 1. LOGIC TABLE(1)

BIAS-1	BIAS-2	FUNCTION	DESCRIPTION
0	0	Full bias mode	Amplifiers ON with lowest distortion possible (default state)
1	0	Mid bias mode	Amplifiers ON with power savings with a reduction in distortion performance
0	1	Low bias mode	Amplifiers ON with enhanced power savings and a reduction of performance
1	1	Shutdown mode	Amplifiers OFF and output has high impedance

(1) Logic pins should not be left floating and should be held at a logic-0 or a logic-1 by external circuitry.

ELECTRICAL CHARACTERISTICS

V_S = ±5 V: R_F = 3 kΩ, R_L = 50 Ω, G = 5, R_{adj} = 0, full bias (unless otherwise noted). Each amplifier independently tested

PARAMETER	CONDITIONS	TYP	OVER TEMPERATURE				
		25°C	25°C	0°C to 70°C	–40°C to 85°C	UNITS	MIN/ MAX
AC PERFORMANCE							
Small-signal bandwidth, – 3 dB (V_O = 100 mVpp)	G = +1, R_F = 4 kΩ	55				MHz	Typ
	G = +2, R_F = 3.5 kΩ	45				MHz	Typ
	G = +5, R_F = 3 kΩ	35				MHz	Typ
	G = +10, R_F = 3 kΩ	25				MHz	Typ
0.1-dB bandwidth flatness	G = +5	7				MHz	Typ
Large-signal bandwidth	G = +5, V_O = 4 Vpp	27				MHz	Typ
Slew rate (25% to 75% level)	G = +5, V_O = 4-V Step, Single-ended	275				V/µs	Typ
	G = +5, V_O = 4-V Step, Differential	450				V/µs	Typ
Rise and fall time	G = +5, V_O = 2-Vpp	10				ns	Typ
Harmonic distortion, 2nd harmonic	G = +5, V_O = 2 Vpp, f = 1 MHz, Differential, R_L = 100 Ω	–88				dBc	Typ
	R_L = 50 Ω	–86				dBc	Typ
Harmonic distortion, 3rd harmonic	R_L = 100 Ω	–83				dBc	Typ
	R_L = 50 Ω	–76				dBc	Typ
Harmonic distortion, 2nd harmonic	G = +5, V_O = 2 Vpp, f = 4 MHz, Differential, R_L = 100 Ω	–84				dBc	Typ
	R_L = 50 Ω	–81				dBc	Typ
Harmonic distortion, 3rd harmonic	R_L = 100 Ω	–62				dBc	Typ
	R_L = 50 Ω	–53				dBc	Typ
Input voltage noise	f > 10 kHz	3				nV/√Hz	Typ
Inverting current noise	f > 10 kHz	5.9				pA/√Hz	Typ
Noninverting current noise	f > 10 kHz	1.2				pA/√Hz	Typ
DC PERFORMANCE							
Open-loop transimpedance gain	R_L = 100 Ω	5				MΩ	Typ
Input offset voltage		±9	±21	±24	±24	mV	Max
Average offset voltage drift		±7				µV/°C	Typ
Input offset voltage matching	Channels 1 to 2 and 3 to 4 only	±0.5	±3	±5	±5	mV	Max
Noninverting input bias current		±1	±10	±15	±15	µA	Max
Noninverting input bias current drift		±150				nA/°C	Typ
Inverting input bias current		±1	±10	±15	±15	µA	Max
Inverting input bias current drift		±150				nA/°C	Typ
INPUT CHARACTERISTICS							
Common-mode input range	RHF package	±4.4	±3.9	±3.8	±3.8	V	Min
	PWP package	±3.5	±2.5	±2.4	±2.4	V	Min
Common-mode rejection ratio		65	58	56	56	dB	Min
Noninverting Input resistance		500‖2				kΩ‖pF	Typ
Inverting input resistance		180				Ω	Typ
OUTPUT CHARACTERISTICS							
Output voltage swing	R_L = 100 Ω	4.1				V	Typ
		–4.1				V	Typ
	R_L = 50 Ω	4	3.8	3.7	3.7	V	Min
		–4	–3.8	–3.7	–3.7	V	Max
	R_L = 25 Ω	4	3.7	3.6	3.6	V	Min
		–4	–3.7	–3.6	–3.6	V	Max
Output current (sourcing)	R_L = 5 Ω	400				mA	Typ
Output current (sinking)	R_L = 5 Ω	400				mA	Typ
Short-circuit output current		±750				mA	Typ
Output impedance	f = 1 MHz	0.2				Ω	Typ

ELECTRICAL CHARACTERISTICS (continued)

V_S = ±5 V: R_F = 3 kΩ, R_L = 50 Ω, G = 5, R_{adj} = 0, full bias (unless otherwise noted). Each amplifier independently tested

PARAMETER	CONDITIONS		TYP	OVER TEMPERATURE				
			25°C	25°C	0°C to 70°C	–40°C to 85°C	UNITS	MIN/ MAX
Crosstalk	f = 1 MHz, Vo = 2 Vpp	D1 to D2, D3 to D4	–35				dB	Typ
		D1 to D3, D2 to D4	–70				dB	Typ
POWER SUPPLY								
Maximum operating voltage				±16	±16	±16	V	Max
Minimum operating voltage				±4	±4	±4	V	Min
Maximum Is+ quiescent current	Per amplifier, Full (Bias-1 = 0, Bias-2 = 0)		3.9	4.4	4.5	4.6	mA	Max
	Per amplifier, Mid (Bias-1 = 1, Bias-2 = 0)		2.9				mA	Typ
	Per amplifier, Low (Bias-1 = 0, Bias-2 = 1)		2					
	Per amplifier, Off (Bias-1 = 1, Bias-2 = 1)		0.2					
Minimum Is+ quiescent current	Per amplifier, Full (Bias-1 = 0, Bias-2 = 0)		3.9	3.2	3	3	mA	Min
Maximum Is– quiescent current	Per amplifier, Full (Bias-1 = 0, Bias-2 = 0)		3.7	4.2	4.3	4.4	mA	Max
	Per amplifier, Mid (Bias-1 = 1, Bias-2 = 0)		2.7				mA	Typ
	Per amplifier, Low (Bias-1 = 0, Bias-2 = 1)		1.8					
	Per amplifier, Off (Bias-1 = 1, Bias-2 = 1)		0.01					
Minimum Is- quiescent current	Per amplifier, Full Bias		3.7	3.1	2.9	2.9	mA	Min
Current through GND pin	Per amplifier, Full (Bias-1 = 0, Bias-2 = 0)		0.2				mA	Typ
Power supply rejection (+PSRR)	V_{S+} = 6 V to 4 V, V_{S-} = –5 V		76	70	68	67	dB	Min
Power supply rejection (–PSRR)	V_{S+} = 5 V, V_{S-} = –6 V to –4 V		70	64	62	61	dB	Min
LOGIC CHARACTERISTICS								
Bias control pin logic threshold	Logic 1, with respect to GND pin(1)		≥2.6				V	Typ
	Logic 0, with respect to GND pin(1)		≤0.8				V	Typ
Bias pin quiescent current	Bias-X = 0.5 V (Logic 0)		1	10	15	15	μA	Max
	Bias-X = 3.3 V (Logic 1)		10	20	30	30		
Turn on time delay($t_{(ON)}$)	Time for I_S to reach 50% of final value		1				μs	Typ
Turn off time delay ($t_{(Off)}$)			1					
Bias pin input impedance			50				kΩ	Typ
Amplifier output impedance	Off (Bias-1 = 1, bias-2 = 1)		10||5				kΩ||pF	Typ

(1) GND pin useable range is from V_{S-} to (V_{S+}– 2.5 V).

Table 2. LOGIC TABLE(1)

BIAS-1	BIAS-2	FUNCTION	DESCRIPTION
0	0	Full Bias Mode	Amplifiers ON with lowest distortion possible (default state)
1	0	Mid Bias Mode	Amplifiers ON with power savings with a reduction in distortion performance
0	1	Low Bias Mode	Amplifiers ON with enhanced power savings and a reduction of performance
1	1	Shutdown Mode	Amplifiers OFF and output has high impedance

(1) Logic pins should not be left floating and should be held by external circuitry to a logic-1 or a logic-0.

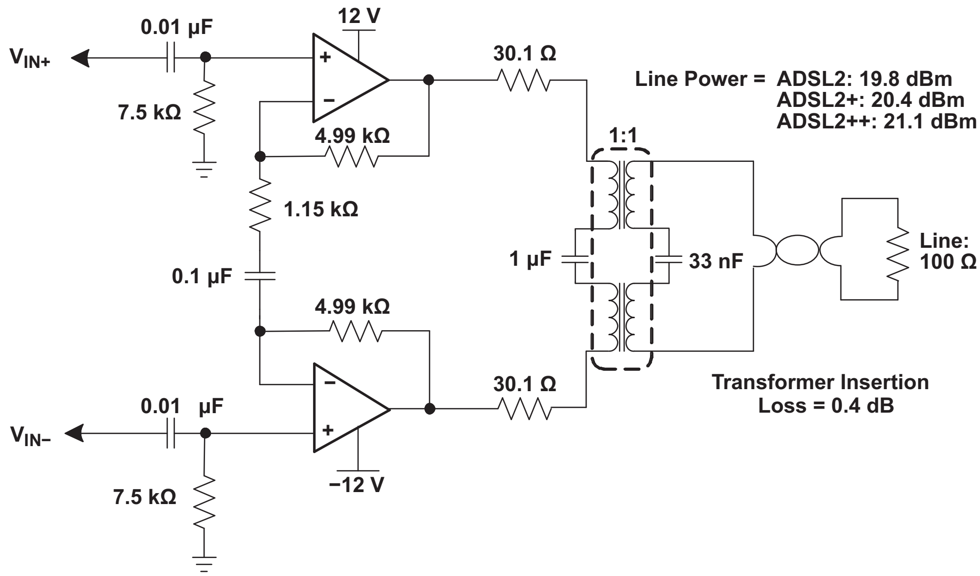


Figure 2. MTPR Test Circuit

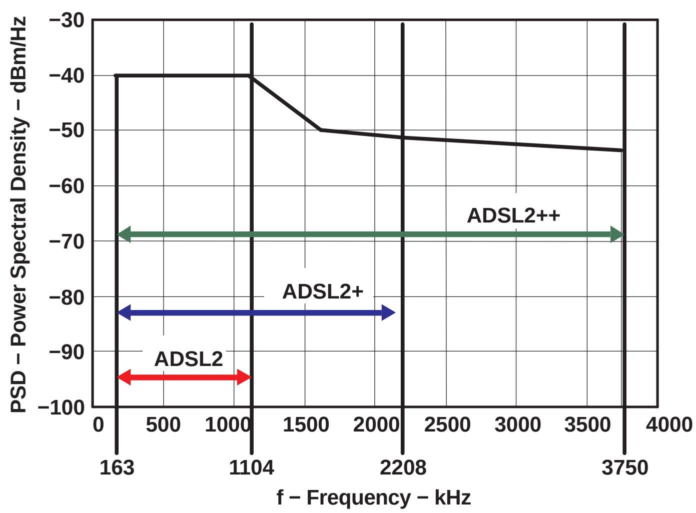


Figure 3. Typical ADSL Line Driver Transmit Frequencies

TYPICAL CHARACTERISTICS

Table 3. Table of Graphs ±12-V Operation

GRAPH TITLE		CONDITIONS	FIGURE
Small Signal Single-Ended Frequency Response		G = 10, R_L = 50 Ω, V_O = 200 mV_{PP}	4
		G = 10, R_L = 100 Ω, V_O = 200 mV_{PP}	5
Large Signal Single-Ended Output Response, Full Bias	vs Frequency	G = 10, R_L = 50 Ω	6
		G = 5, R_L = 50 Ω	7
Small Signal Differential Frequency Response		G = 5, R_L = 50 Ω, V_O = 200 mV_{PP}	8
Large Signal Differential Output Response, Full Bias	vs Frequency	G = 10, R_L = 100 Ω	9
		G = 5, R_L = 100 Ω	10
Differential Harmonic Distortion	vs Frequency	G = 5, R_L = 100 Ω, V_O = $2V_{PP}$, R_F = 3 kΩ, R_G = 1.5kΩ	11
		G = 5, R_L = 50 Ω, V_O = $2V_{PP}$, R_F = 3 kΩ, R_G = 1.5 kΩ	12
		G = 10, R_L = 100 Ω, V_O = $2V_{PP}$, R_F = 3 kΩ, R_G = 665Ω	13
		G = 10, R_L = 50 Ω, V_O = 2 V_{PP}, R_F = 3 kΩ, R_G = 665Ω	14
		G = 10, R_L = 100Ω, V_O = 2 V_{PP}, R_F = 5 kΩ, R_G = 1.1 kΩ	15
		G = 10, R_L = 5 0Ω, V_O = 2 V_{PP}, R_F = 5 kΩ, R_G = 1.1 kΩ	16
Single-Ended 2nd-Order Harmonic Distortion	vs Frequency	G = 5, R_L = 50 Ω, V_O = 2 V_{PP}	17
Single-Ended 3rd-Order Harmonic Distortion			18
Single-Ended 2nd-Order Harmonic Distortion	vs Frequency	G = 10, R_L = 50 Ω, V_O = 2 V_{PP}	19
Single-Ended 3rd-Order Harmonic Distortion			20
Differential Crosstalk—Gain = 10 V/V		G = 10, R_F = 4 kΩ, R_G = 884 Ω, V_S = ±12 V	21
Single-Ended Crosstalk—Gain = 10 V/V		G = 10, R_F = 4 kΩ, R_G = 442 Ω, V_S = ±12 V	22
Single-Ended Crosstalk—Gain = 1 V/V		G = 1, R_F = 4 kΩ, V_S = ±12 V	23
Transimpedance Gain and Phase	vs Frequency	R_L = 100 Ω	24
Input Referred Noise	vs Frequency		25
Small Signal Single-Ended Transient Response	vs Time	G = 5, R_L = 100 Ω, V_O = 200 mV_{PP}	27
Large Signal Single-Ended Transient Response	vs Time	G = 5, R_L = 100 Ω, V_O = 5 V_{PP}	27
Overdrive Recovery	vs Time	G = 5, R_L = 100 Ω	28
Single-Ended Transition Rate	vs Output Voltage	G = 5, R_L = 100 Ω	29
Differential Transition Rate	vs Output Voltage	G = 5, R_L = 100 Ω	30
Positive Output Voltage Headroom	vs Temperature	R_L = 100 Ω	31
Negative Output Voltage Headroom	vs Temperature	R_L = 100 Ω	32
Input Offset Voltage	vs Supply Voltage		33
	vs Free-Air Temperature		34
	vs Input Common-Mode Range		35
Input Bias Current	vs Supply Voltage		36
Single-Ended Rejection Ratios	vs Frequency	G = 2, R_L = 50 Ω	37
Differential Rejection Ratio	vs Frequency	G = 10, R_L = 100 Ω	38
Output Impedance	vs Frequency	G = 10	39
		G = 5	40

Table 4. Table of Graphs ±5-V Operation

GRAPH TITLE		CONDITIONS	FIGURE
Large Signal Single-Ended Output Response, Full Bias	vs Frequency	G = 5, R_L = 50 Ω, V_O = 0.25 V_{PP} – 4 V_{PP}	41
Large Signal Differential Output Response, Full Bias	vs Frequency	G = 5, R_L = 100 Ω, V_O = 0.25 V_{PP} – 8 V_{PP}	42
Differential Harmonic Distortion	vs Frequency	G = 5, R_L = 100 Ω, V_O = 2 V_{PP}	43
		G = 5, R_L = 50 Ω, V_O = 2 V_{PP}	44
		G = 10, R_L = 100 Ω, V_O = 2 V_{PP}	45
		G = 10, R_L = 50 Ω, V_O = 2 V_{PP}	46
Transimpedance Gain and Phase	vs Frequency	R_L = 100 Ω	47
Single-Ended Transition Rate	vs Output Voltage	G = 5, R_L = 100 Ω	48
Differential Transition Rate	vs Output Voltage	G = 5, R_L = 100 Ω	49
Output Impedance	vs Frequency	G = 5	50

SMALL SIGNAL SINGLE-ENDED FREQUENCY RESPONSE, G=10, R_L = 50Ω

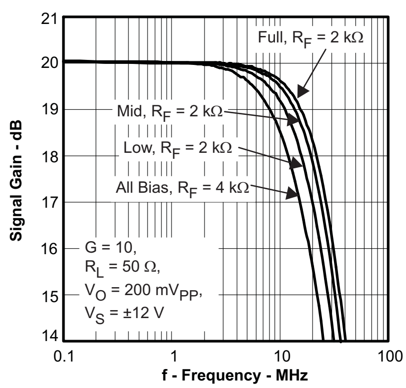


Figure 4.

SMALL-SIGNAL SINGLE-ENDED FREQUENCY RESPONSE, G=10, R_L = 100Ω

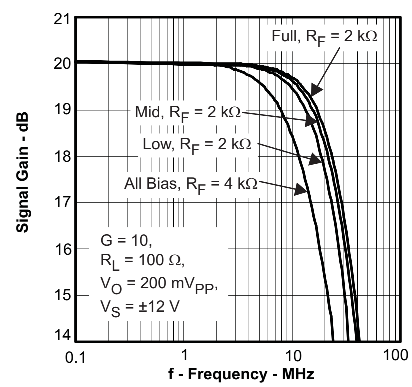


Figure 5.

LARGE SIGNAL SINGLE-ENDED OUTPUT RESPONSE, FULL BIAS vs FREQUENCY, G = 10, R_L = 50Ω

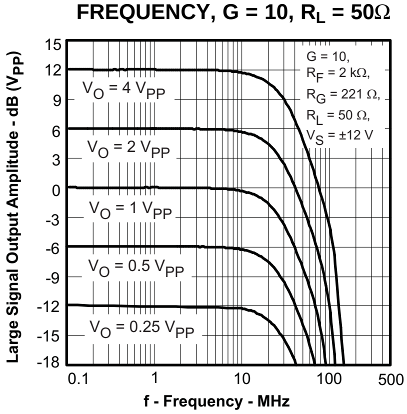


Figure 6.

LARGE SIGNAL SINGLE-ENDED OUTPUT RESPONSE, FULL BIAS vs FREQUENCY, G = 5, R_L = 50Ω

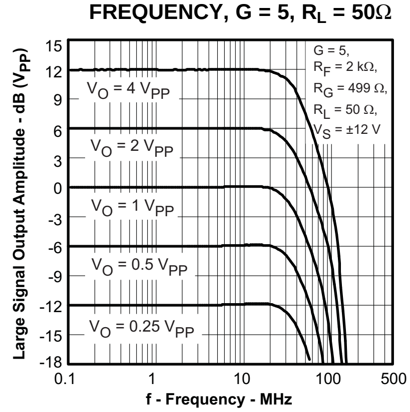


Figure 7.

SMALL SIGNAL DIFFERENTIAL
FREQUENCY RESPONSE, G = 5, R_L = 50Ω

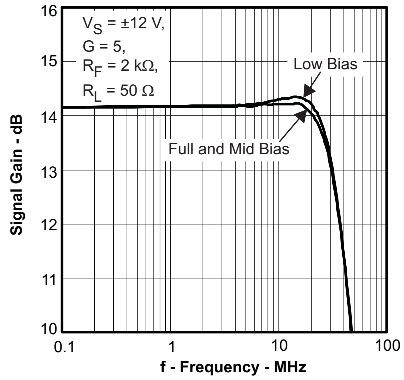


Figure 8.

LARGE SIGNAL DIFFERENTIAL
OUTPUT RESPONSE, FULL BIAS
vs
FREQUENCY, G = 10, R_L = 100Ω

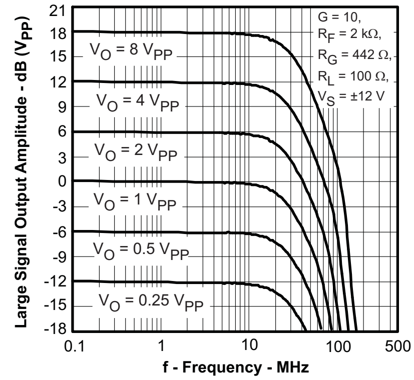


Figure 9.

LARGE SIGNAL DIFFERENTIAL
OUTPUT RESPONSE, FULL BIAS
vs
FREQUENCY, G = 5, R_L = 100Ω

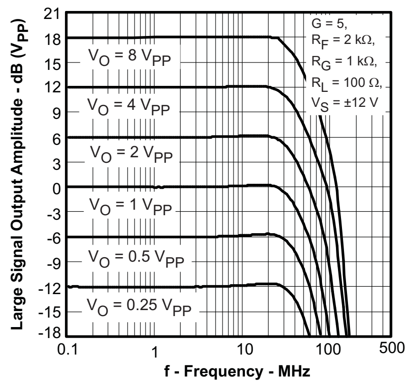


Figure 10.

DIFFERENTIAL HARMONIC DISTORTION
vs
FREQUENCY, G = 5, R_L = 100Ω

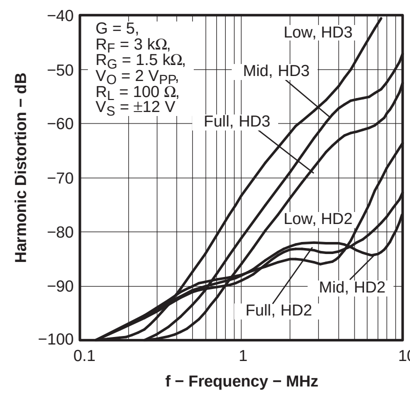


Figure 11.

DIFFERENTIAL HARMONIC DISTORTION
vs
FREQUENCY, G = 5, R_L = 50 Ω

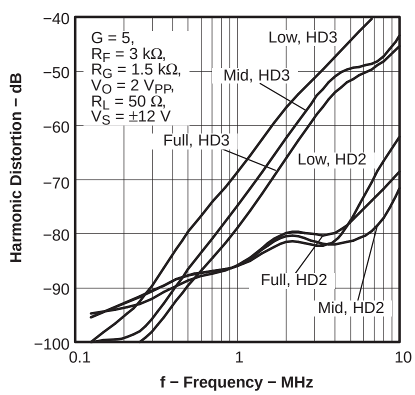


Figure 12.

DIFFERENTIAL HARMONIC DISTORTION
vs
FREQUENCY, G = 10, R_L = 100 Ω

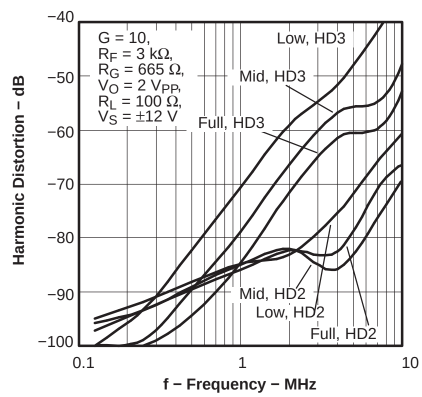


Figure 13.

DIFFERENTIAL HARMONIC DISTORTION vs FREQUENCY, G = 10, R_L = 50 Ω

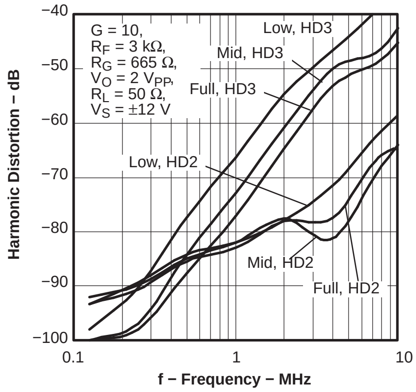


Figure 14.

DIFFERENTIAL HARMONIC DISTORTION vs FREQUENCY, G = 10, R_L = 100 Ω

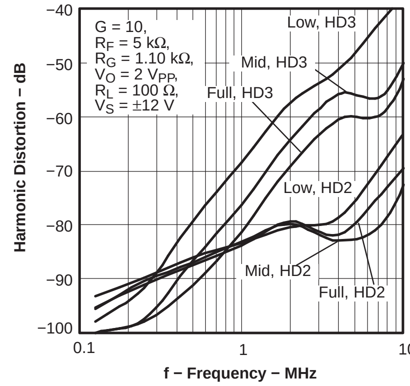


Figure 15.

DIFFERENTIAL HARMONIC DISTORTION vs FREQUENCY, G = 10, R_L = 50 Ω

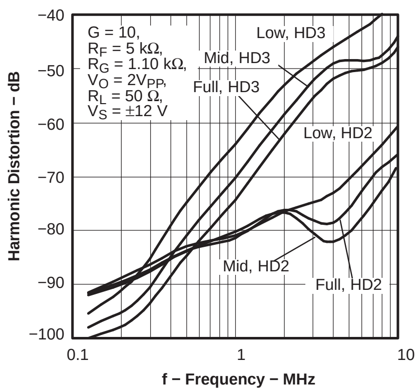


Figure 16.

SINGLE-ENDED 2ND-ORDER HARMONIC DISTORTION vs FREQUENCY, G = 5, R_L = 50Ω

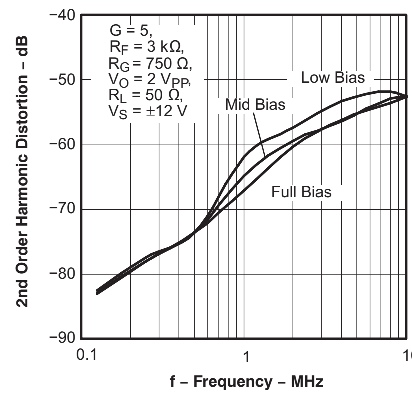


Figure 17.

SINGLE-ENDED 3RD-ORDER HARMONIC DISTORTION vs FREQUENCY, G = 5, R_L = 50Ω

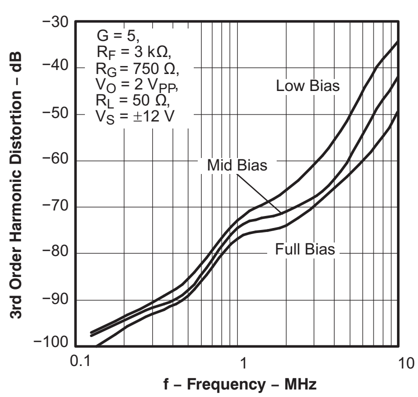


Figure 18.

SINGLE-ENDED 2ND-ORDER HARMONIC DISTORTION vs FREQUENCY, G = 10, R_L = 50Ω

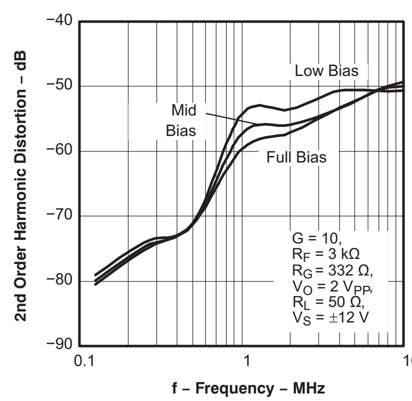


Figure 19.

SINGLE-ENDED 3RD-ORDER HARMONIC DISTORTION vs FREQUENCY, G = 10, R_L = 50Ω

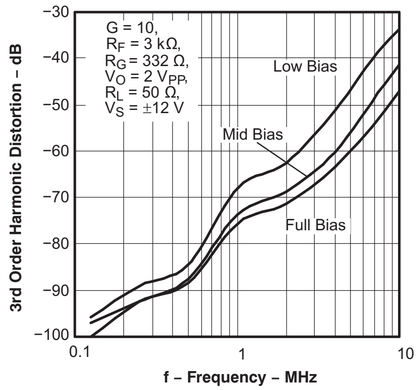


Figure 20.

DIFFERENTIAL CROSSTALK—GAIN = 10 V/V

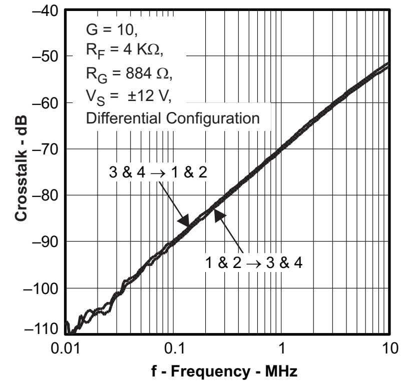


Figure 21.

SINGLE-ENDED CROSSTALK—GAIN = 10 V/V

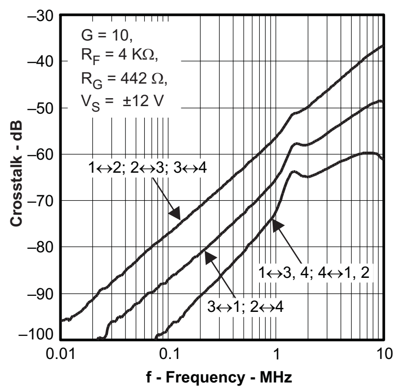


Figure 22.

SINGLE-ENDED CROSSTALK—GAIN = 1 V/V

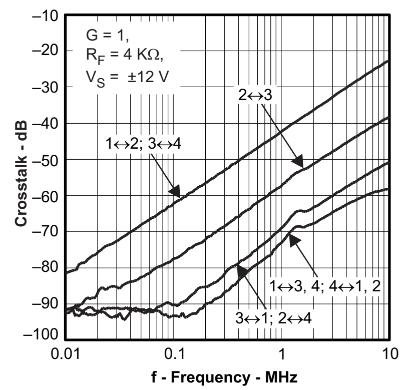


Figure 23.

TRANSIMPEDANCE GAIN AND PHASE vs FREQUENCY

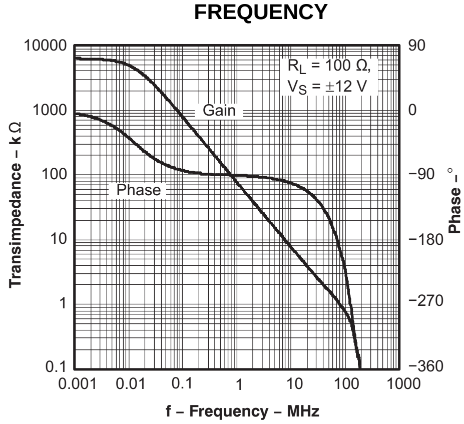


Figure 24.

INPUT REFERRED NOISE vs FREQUENCY

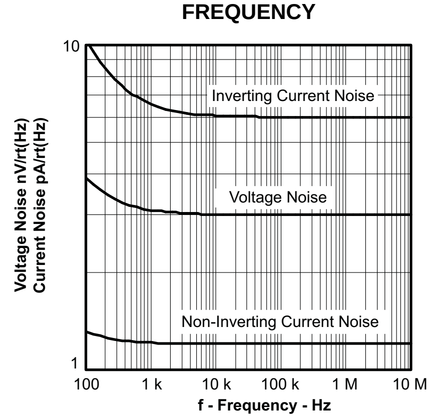


Figure 25.

SMALL SIGNAL SINGLE-ENDED TRANSIENT RESPONSE vs TIME, G = 5, R_L = 100Ω

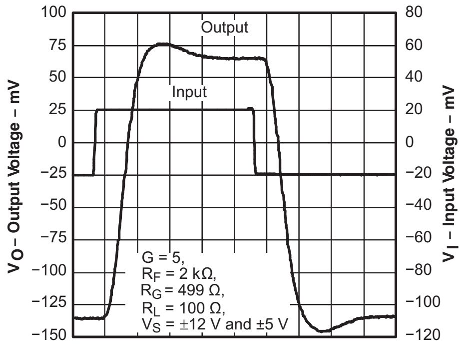


Figure 26.

LARGE SIGNAL SINGLE-ENDED TRANSIENT RESPONSE vs TIME, G = 5, R_L = 100Ω

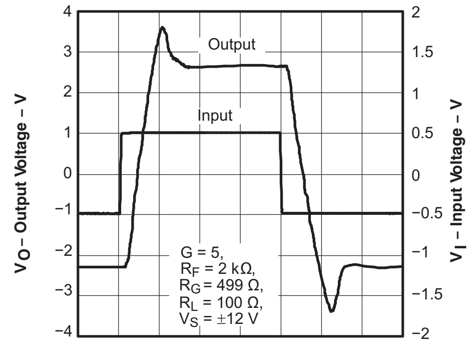


Figure 27.

OVERDRIVE RECOVERY vs TIME, G = 5, R_L = 100Ω

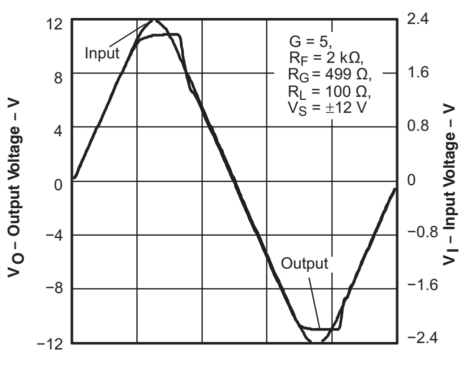


Figure 28.

SINGLE-ENDED TRANSITION RATE vs OUTPUT VOLTAGE, G = 5, R_L = 100Ω

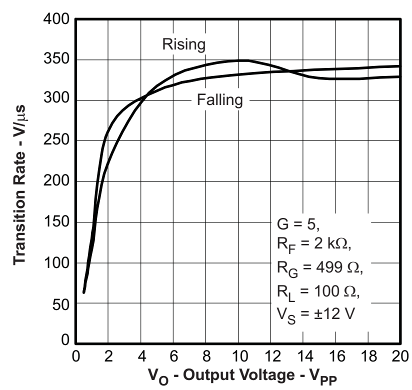


Figure 29.

DIFFERENTIAL TRANSITION RATE vs OUTPUT VOLTAGE, G = 5, R_L = 100Ω

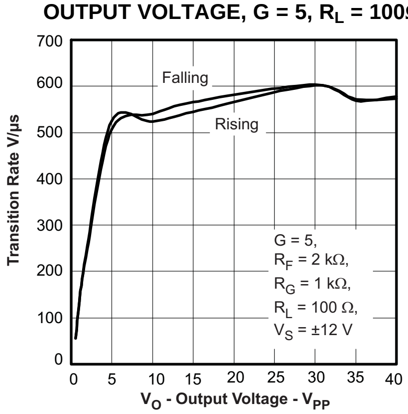


Figure 30.

POSITIVE OUTPUT VOLTAGE HEADROOM vs TEMPERATURE, R_L = 100Ω

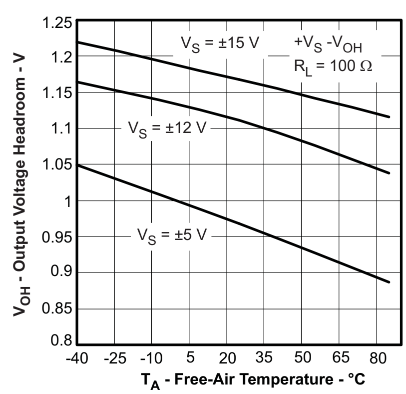


Figure 31.

NEGATIVE OUTPUT VOLTAGE HEADROOM vs TEMPERATURE, R_L = 100Ω

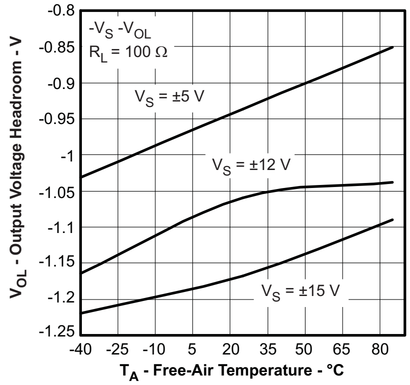


Figure 32.

INPUT OFFSET VOLTAGE vs SUPPLY VOLTAGE

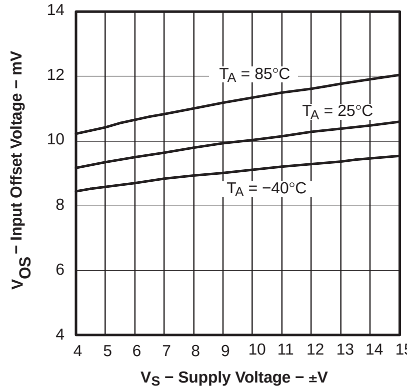


Figure 33.

INPUT OFFSET VOLTAGE vs FREE-AIR TEMPERATURE

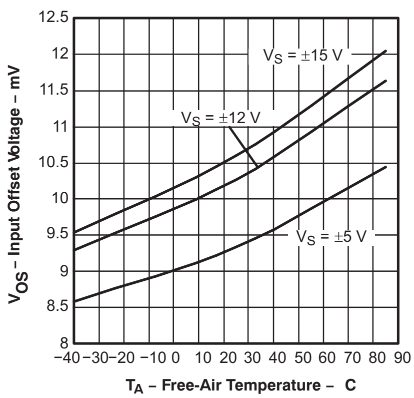


Figure 34.

INPUT OFFSET VOLTAGE vs INPUT COMMON-MODE RANGE

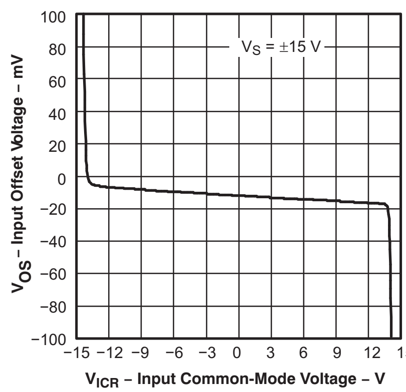


Figure 35.

INPUT BIAS CURRENT vs SUPPLY VOLTAGE

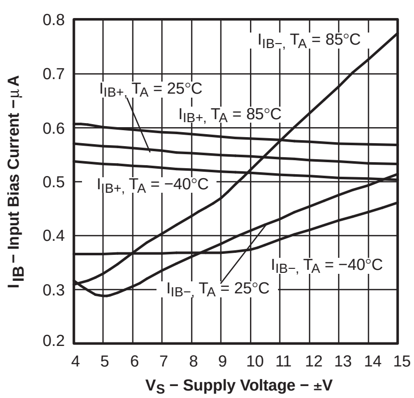


Figure 36.

SINGLE-ENDED REJECTION RATIOS vs FREQUENCY, G = 2, R_L = 50Ω

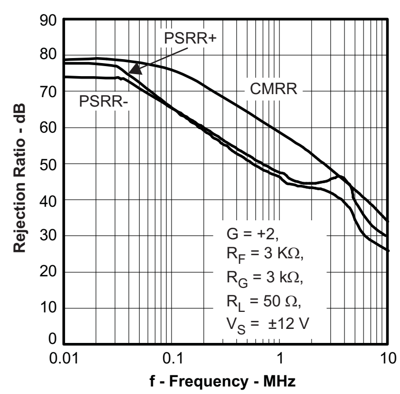


Figure 37.

DIFFERENTIAL REJECTION RATIO vs FREQUENCY, G = 10, R_L = 100Ω

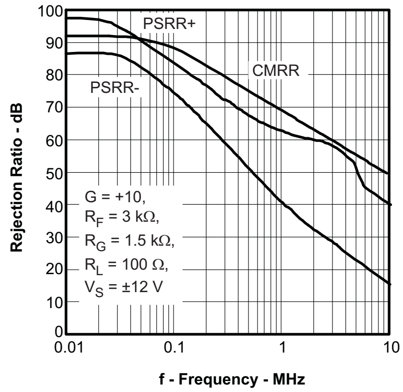


Figure 38.

OUTPUT IMPEDANCE vs FREQUENCY, G = 10

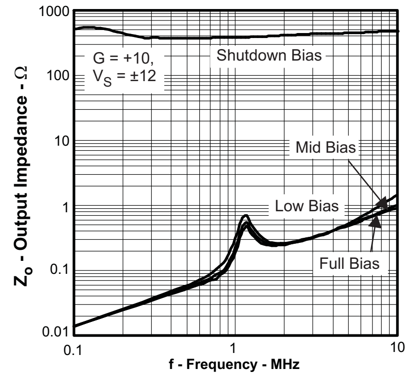


Figure 39.

OUTPUT IMPEDANCE vs FREQUENCY, G = 5

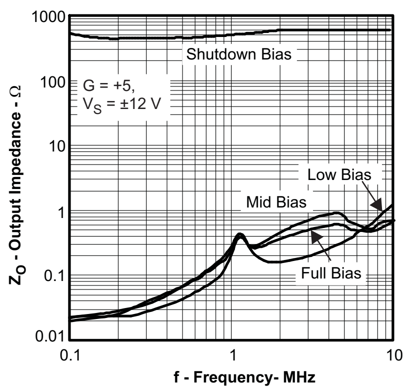


Figure 40.

LARGE SIGNAL SINGLE-ENDED OUTPUT RESPONSE, FULL BIAS vs FREQUENCY, G = 5, R_L = 50Ω

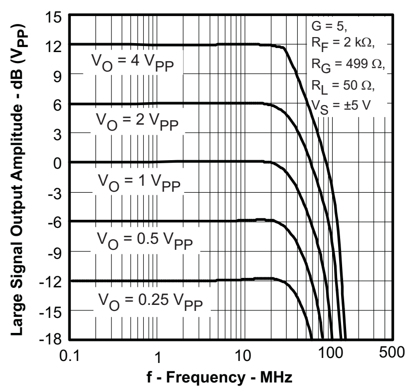


Figure 41.

LARGE SIGNAL DIFFERENTIAL OUTPUT RESPONSE, FULL BIAS vs FREQUENCY, G = 5, R_L = 50Ω

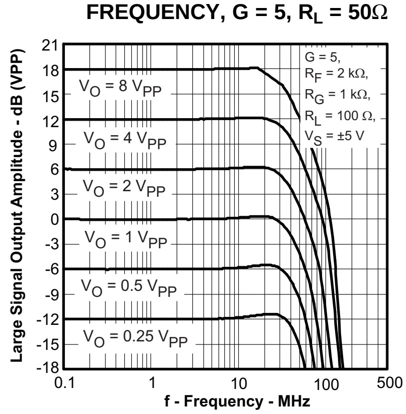


Figure 42.

DIFFERENTIAL HARMONIC DISTORTION vs FREQUENCY, G = 5, R_L = 100Ω

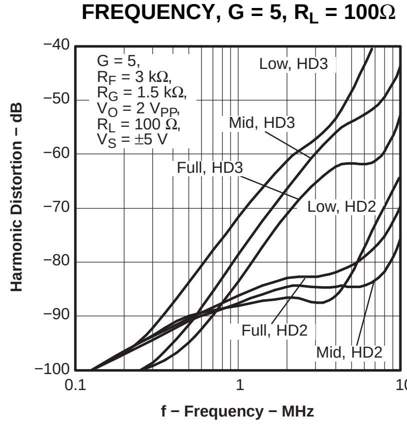


Figure 43.

DIFFERENTIAL HARMONIC DISTORTION vs FREQUENCY, G = 5, R_L = 50Ω

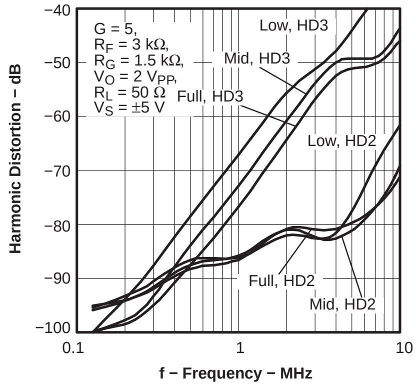


Figure 44.

DIFFERENTIAL HARMONIC DISTORTION vs FREQUENCY, G = 10, R_L = 100Ω

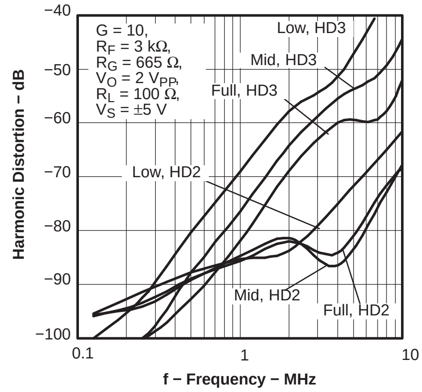


Figure 45.

DIFFERENTIAL HARMONIC DISTORTION vs FREQUENCY, G = 10, R_L = 50Ω

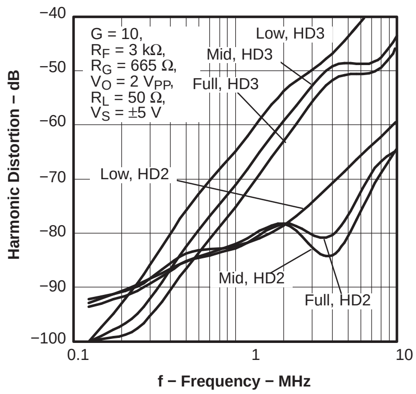


Figure 46.

TRANSIMPEDANCE GAIN AND PHASE vs FREQUENCY, R_L = 100Ω

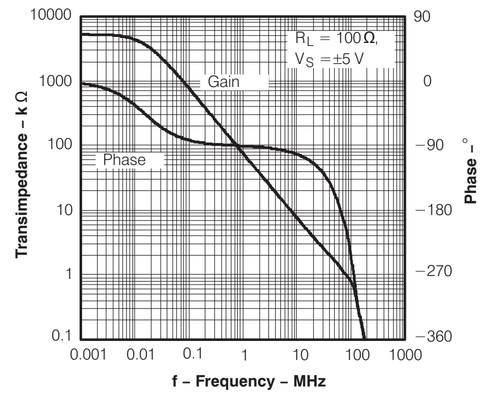


Figure 47.

SINGLE-ENDED TRANSITION RATE vs OUTPUT VOLTAGE, G = 5, R_L = 100Ω

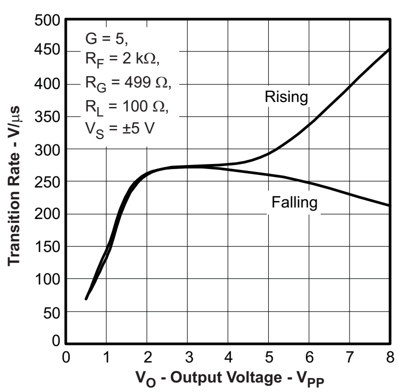


Figure 48.

DIFFERENTIAL TRANSITION RATE vs OUTPUT VOLTAGE, G = 5, R_L = 100Ω

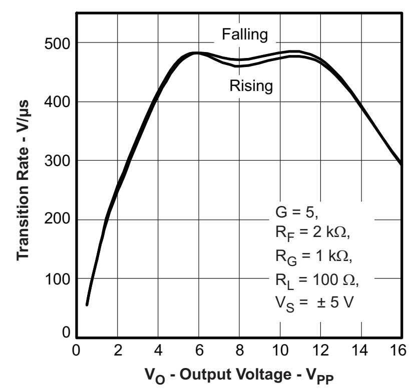


Figure 49.

**OUTPUT IMPEDANCE
vs
FREQUENCY, G = 5**

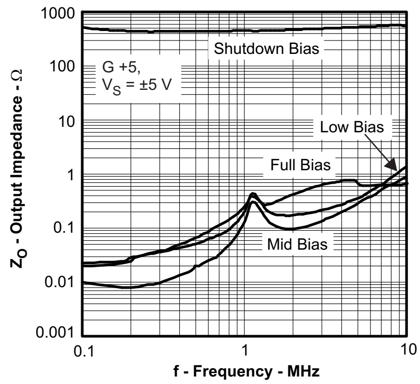


Figure 50.

APPLICATION INFORMATION

The THS6184 contains four independent operational amplifiers. These amplifiers are current feedback topology amplifiers made for high-speed operation. They have been specifically designed to deliver the full power requirements of ADSL and therefore can deliver output currents of at least 400 mA at full output voltage.

The THS6184 is fabricated using Texas Instruments 36-V complementary bipolar process, BiCOM1. This process provides exceptional device speed with high breakdown voltages.

DEVICE PROTECTION FEATURE

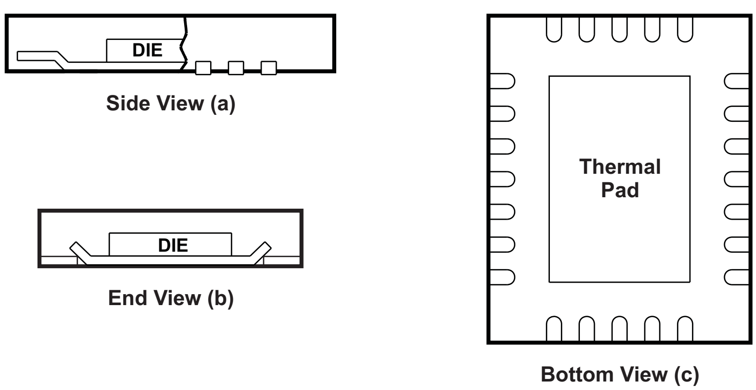
The THS6184 has a built-in thermal protection feature. Should the internal junction temperature rise above approximately 160°C, the device automatically shuts down. Such a condition could exist with improper heat sinking or if the output is shorted to ground. When the abnormal condition is fixed, the internal thermal shutdown circuit automatically turns the device back on. This occurs at approximately 145°C, junction temperature. Note that the THS6184 does not have short-circuit protection and care should be taken to minimize the output current below the absolute maximum ratings.

THERMAL INFORMATION

The THS6184 is available in thermally-enhanced RHF and PWP packages, which are members of the PowerPAD family of packages. These packages are constructed using leadframes upon which the dies are mounted [see Figure 51 for the RHF package and Figure 52 for the PWP package]. This arrangement results in the lead frames being exposed as thermal pads on the underside of their respective packages. Because a thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad. Note that the PowerPAD is electronically isolated from the active circuitry and any pins. Thus, the PowerPAD can be connected to any potential voltage within the absolute maximum voltage range. Ideally, connection of the PAD to the ground plane is preferred as the plane typically is the largest copper plane on a PCB.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device. This is discussed in more detail in the *PCB design considerations section* of this document.

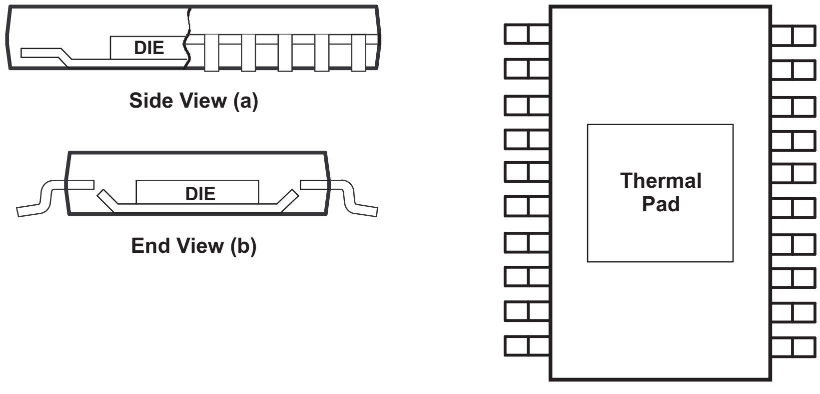
The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with the, heretofore, awkward mechanical methods of heatsinking.



A. The thermal pad is electrically isolated from all terminals in the package.

Figure 51. Views of Thermally Enhanced RHF Package (Representative Only – Not to Scale)

APPLICATION INFORMATION (continued)



A. The thermal pad is electrically isolated from all terminals in the package.

Figure 52. Views of Thermally Enhanced PWP Package (Representative Only – Not to Scale)

RECOMMENDED FEEDBACK AND GAIN RESISTOR VALUES

As with all current feedback amplifiers, the bandwidth of the THS6184 is an inversely proportional function of the value of the feedback resistor. The recommended resistors with a ±12-V power supply for the optimum frequency response with a 100-Ω load system is 2 kΩ for a gain of 5. These should be used as a starting point and once optimum values are found, 1% tolerance resistors should be used to maintain frequency response characteristics.

Consistent with current feedback amplifiers, increasing the gain is best accomplished by changing the gain resistor, not the feedback resistor. This is because the bandwidth of the amplifier is dominated by the feedback resistor value and internal dominant-pole capacitor. The ability to control the amplifier gain independently of the bandwidth constitutes a major advantage of current feedback amplifiers over conventional voltage feedback amplifiers.

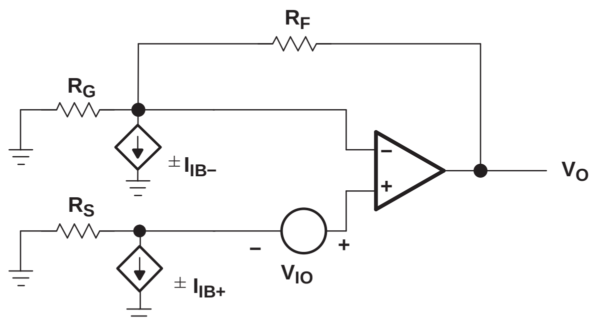
It is important to realize the effects of the feedback resistance on distortion. Increasing the resistance decreases the loop gain and increases the distortion. It is also important to know that decreasing load impedance increases total harmonic distortion (THD). Typically, the third order harmonic distortion increases more than the second order harmonic distortion.

Finally, in a differential configuration as shown in Figure 1, it is important to note that there is a differential gain and a common-mode gain which are different from each other. Differentially, the gain is at $1 + 2R_F/R_G$. While common-mode gain = 1 due to R_G being connected directly between each amplifier and not to ground.

APPLICATION INFORMATION (continued)

OFFSET VOLTAGE

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:



$$V_{OO} = V_{IO}\left(1 + \frac{R_F}{R_G}\right) \pm I_{IB+}\, R_S\left(1 + \frac{R_F}{R_G}\right) \pm I_{IB-}\, R_F$$

Figure 53. Output Offset Voltage Model

NOISE CALCULATIONS

Noise can cause errors on very small signals. This is especially true for the amplifying small signals. The noise model for current feedback amplifiers (CFB) is the same as voltage feedback amplifiers (VFB). The only difference between the two is that the CFB amplifiers generally specify different current noise parameters for each input while VFB amplifiers usually only specify one noise current parameter. The noise model is shown in Figure 54. This model includes all of the noise sources as follows:

- e_n = Amplifier internal voltage noise (nV/$\sqrt{Hz}$)
- IN+ = Noninverting current noise (pA/$\sqrt{Hz}$)
- IN- = Inverting current noise (pA/$\sqrt{Hz}$)
- e_{RX} = Thermal voltage noise associated with each resistor ($e_{RX} = \sqrt{4\ kTR_x}$)

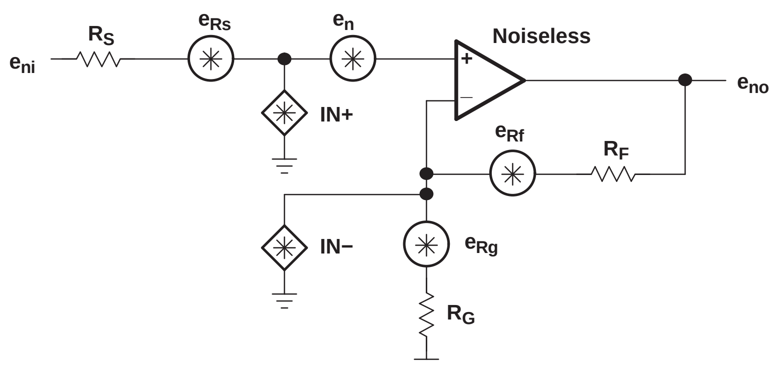


Figure 54. Noise Model

APPLICATION INFORMATION (continued)

The total equivalent input noise density (e_{ni}) is calculated by using the following equation:

$$e_{ni} = \sqrt{\left(e_n\right)^2 + \left(IN+ \times R_S\right)^2 + \left(IN- \times \left(R_F \parallel R_G\right)\right)^2 + 4\,kTR_S + 4\,kT\left(R_F \parallel R_G\right)}$$

Where:

k = Boltzmann's constant = 1.380658×10^{-23}
T = Temperature in degrees Kelvin (273 +°C)
R_F || R_G = Parallel resistance of R_F and R_G

To get the equivalent output noise of the amplifier, just multiply the equivalent input noise density (e_{ni}) by the overall amplifier gain (A_V).

$$e_{no} = e_{ni}\,A_V = e_{ni}\left(1 + \frac{R_F}{R_G}\right) \text{ (Noninverting Case)}$$

As the previous equations show, to keep noise at a minimum, small value resistors should be used. As the closed-loop gain is increased (by reducing R_G), the input noise is reduced considerably because of the parallel resistance term.

DRIVING A CAPACITIVE LOAD

Driving capacitive loads with high performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS6184 has been internally compensated to maximize its bandwidth and slew rate performance at low quiescent current. When the amplifier is compensated in this manner, capacitive loading directly on the output decreases the device's phase margin leading to high-frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 55. A minimum value of 2 Ω should work well for most applications.

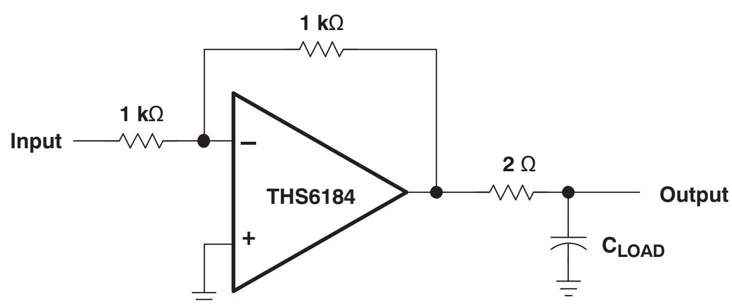
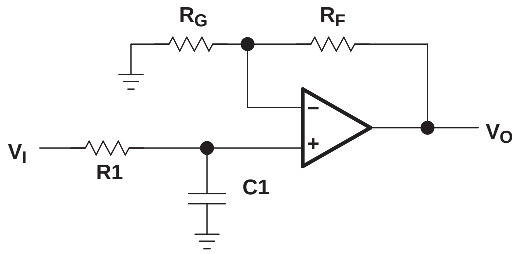


Figure 55. Driving a Capacitive Load

GENERAL CONFIGURATIONS

A common error for the first-time CFB user is to create a unity gain buffer amplifier by shorting the output directly to the inverting input. A CFB amplifier in this configuration oscillates and is **not** recommended. The THS6184, like all CFB amplifiers, **must** have a feedback resistor for stable operation. Additionally, placing capacitors directly from the output to the inverting input is not recommended. This is because, at high frequencies, a capacitor has a very low impedance. This results in an unstable amplifier and should not be considered when using a current-feedback amplifier. Because of this, integrators and simple low-pass filters, which are easily implemented on a VFB amplifier, have to be designed slightly differently. If filtering is required, simply place an RC-filter at the noninverting terminal of the operational-amplifier (see Figure 56).

APPLICATION INFORMATION (continued)

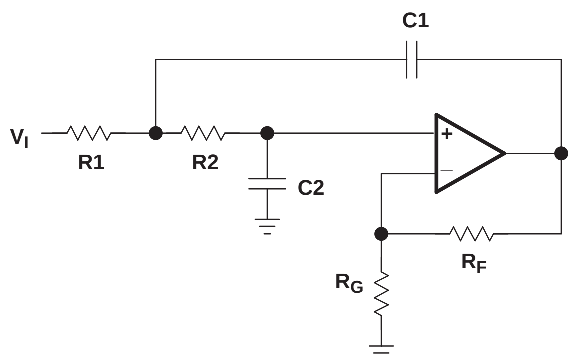


$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR1C1}\right)$$

$$f_{-3dB} = \frac{1}{2\pi R1C1}$$

Figure 56. Single-Pole Low-Pass Filter

If a multiple pole filter is required, the use of a Sallen-Key filter can work very well with CFB amplifiers. This is because the filtering elements are not in the negative feedback loop and stability is not compromised. Because of their high slew-rates and high bandwidths, CFB amplifiers can create very accurate signals and help minimize distortion. An example is shown in Figure 57.



R1 = R2 = R
C1 = C2 = C
Q = Peaking Factor
(Butterworth Q = 0.707)

$$f_{-3dB} = \frac{1}{2\pi RC}$$

$$R_G = \frac{R_F}{\left(2 - \frac{1}{Q}\right)}$$

Figure 57. 2-Pole Low-Pass Sallen-Key Filter

PCB DESIGN CONSIDERATIONS

Proper PCB design techniques in two areas are important to assure proper operation of the THS6184. These areas are high-speed layout techniques and thermal-management techniques. Because the THS6184 is a high-speed part, the following guidelines are recommended.

- Ground plane – It is essential that a ground plane be used on the board to provide all components with a low inductive ground connection. Although a ground connection directly to a terminal of the THS6184 is not necessarily required, it is recommended that the thermal pad of the package be tied to ground. This serves two functions. It provides a low inductive ground to the device substrate to minimize internal crosstalk and it provides the path for heat removal. Note that the BiCOM1 process is an SOI process and thus, the substrate is isolated from the active circuitry.
- Input stray capacitance – To minimize potential problems with amplifier oscillation, the capacitance at the inverting input of the amplifiers must be kept to a minimum. To do this, PCB trace runs to the inverting input must be as short as possible, the ground plane should be removed under any etch runs connected to the inverting input, and external components should be placed as close as possible to the inverting input. This is especially true in the noninverting configuration.
- Proper power supply decoupling – Use a minimum of a 6.8-µF tantalum capacitor in parallel with a 0.1-µF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-µF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-µF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting etch makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminal and the ceramic capacitors.
- For a differential configuration as shown in Figure 1, it is recommended that a 0.1-µF or 1-µF capacitor be

APPLICATION INFORMATION (continued)

added across the power supplies (from V_{CC+} to V_{CC-}) as close as possible to the THS6184. This allows for differential currents to flow properly, slightly reducing even-order harmonic distortion. The 0.1-µF capacitors to ground should also be used as previously stipulated.

Because of its high power delivery, proper thermal management of the THS6184 is required. Although there are many ways to properly heatsink this device, the following steps illustrate one recommended approach for a multilayer PCB with an internal ground plane utilizing the 24-pin RHF, (or the 20-pin PWP) PowerPAD package.

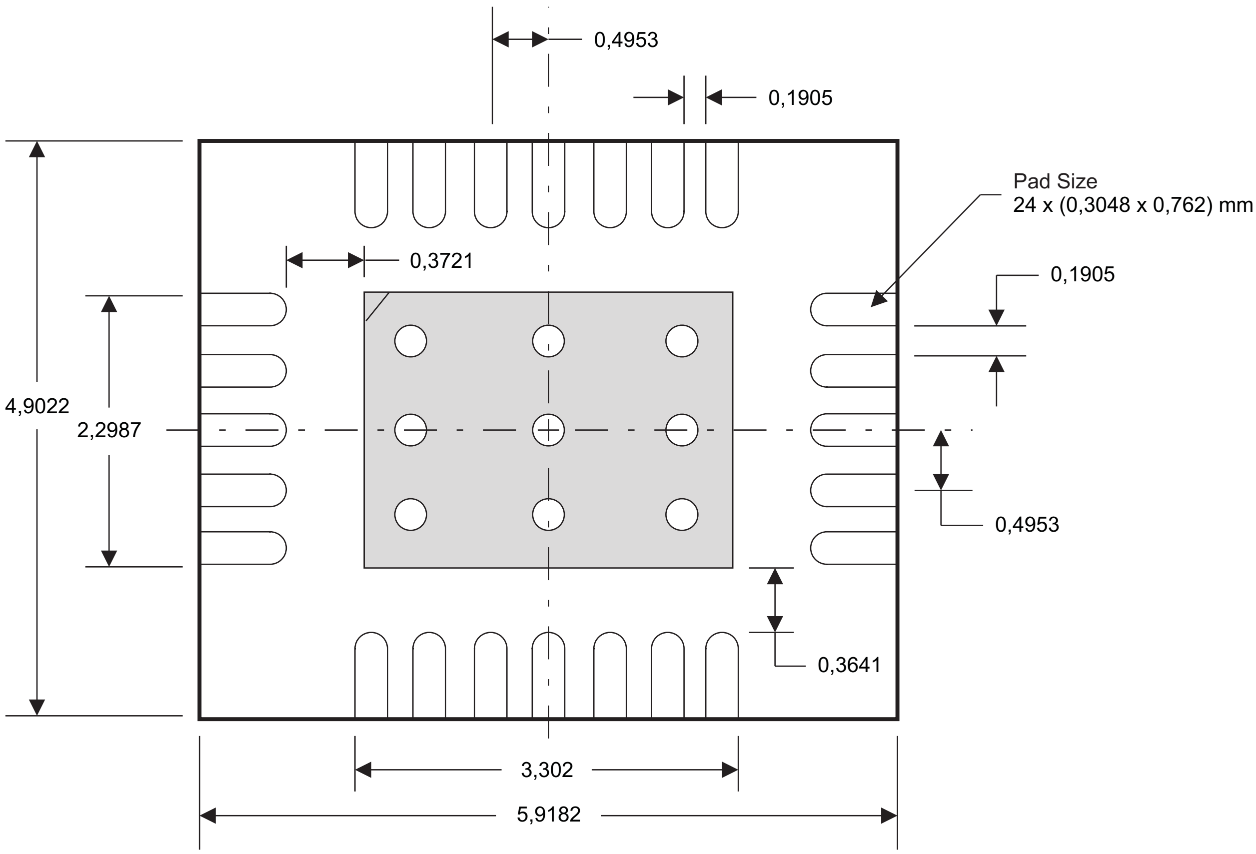
1. Prepare the PCB with a top-side etch pattern to accommodate an RHF package as shown in Figure 58. If the PWP package is to be used, prepare the PCB etch pattern as shown in Figure 59. There should be etch for the leads as well as etch for the thermal pad.
2. PCB vias in the area of the thermal pad should be kept small so that solder wicking through the holes is not a problem during reflow. All of the vias in the thermal pad should connected to the internal PCB ground plane.

a. RHF package – Place 9 holes in the area of the thermal pad. These holes should be 0,254 mm (10 mils) in diameter.

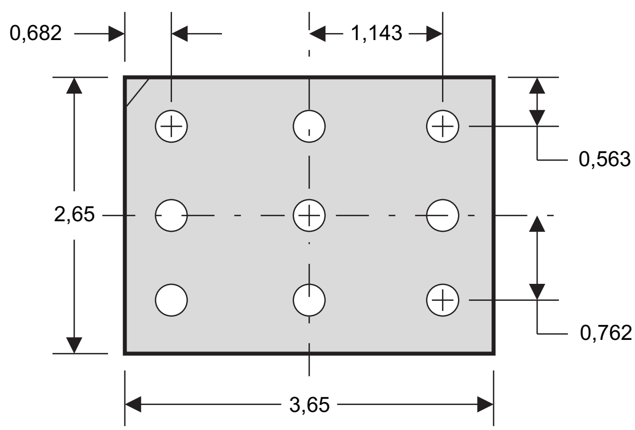
b. PWP package – Place 9 holes in the area of the thermal pad. These holes should be 0,33 mm (13 mils) in diameter.

3. When connecting these holes to the ground plane, do **not** use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. However, in this application, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS6184 package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated through hole.
4. The top-side solder mask should leave the terminals of the package and the thermal pad area with its thermal transfer holes exposed. Any holes outside the thermal pad area, but still under the package, should be covered with solder mask.
5. Apply solder paste to the exposed thermal pad area and all of the operational amplifier terminals.
6. With these preparatory steps in place, the THS6184 RHF is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

APPLICATION INFORMATION (continued)



PowerPAD and Via Layout
(Pad Size 3,65 mm x 2,65 mm. 9 Vias with Diameter = 0,254 mm)



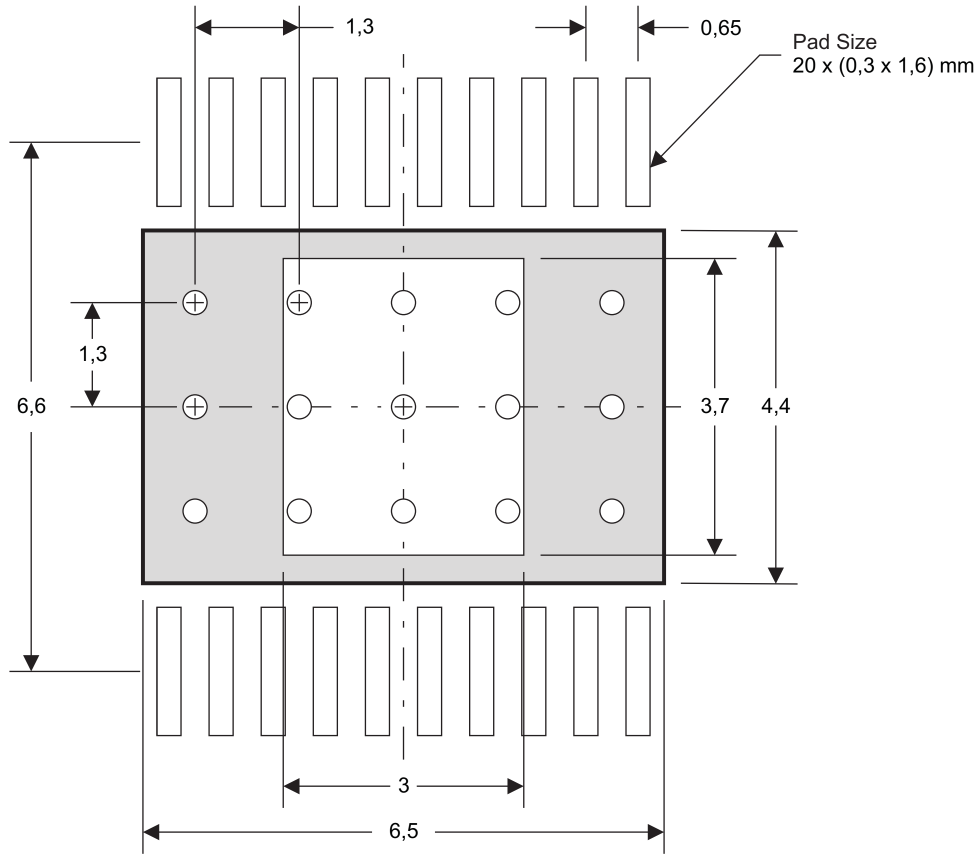
Vias should go through the board connecting the top PowerPAD to any and all ground planes. The larger the ground plane, the more area to distribute the heat.

Solder resist should be used on the bottom side ground plane to prevent wicking of the solder through the vias during the process.

Note: All linear dimensions are in millimeters.

Figure 58. Suggested PCB Layout For 24-Pin RHF Package

APPLICATION INFORMATION (continued)



PowerPAD and Via Layout
(Pad Size 3 mm x 3,7 mm. 9 Vias with Diameter = 0,3 mm)

Vias should go through the board connecting the top PowerPAD to any and all ground planes. The larger the ground plane, the more area to distribute the heat.

Solder resist should be used on the bottom side ground plane to prevent wicking of the solder through the vias during the process.

Note: All linear dimensions are in millimeters.

Figure 59. Suggested PCB Layout For 20-Pin PWP Package

APPLICATION INFORMATION (continued)

The actual thermal performance achieved with the THS6184 in the 24-pin RHF PowerPAD package or the 20-pin PWP PowerPAD package depends on the application. If the size of the internal ground plane is approximately 3 inches × 3 inches, and the chip PowerPAD is soldered to the PCB thermal pad, then the expected thermal coefficient, θ_{JA}, is about 32°C/W for the RHF package, and is 32.6°C/W for the PWP package. (See the Package Dissipation Ratings Table for all other package metrics.) For a given θ_{JA}, the maximum power dissipation is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}}\right)$$

Where:

P_D = Maximum power dissipation of THS6184 (watts)
T_{MAX} = Absolute maximum operating junction temperature (130°C)
T_A = Free-ambient air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$

θ_{JC} = Thermal coefficient from junction to case. See the Package Dissipation Ratings table.
θ_{CA} = Thermal coefficient from case to ambient determined by PCB layout and construction.

More complete details of the PowerPAD installation process and thermal management techniques can be found in the Texas Instruments Technical Brief, *PowerPAD Thermally Enhanced Package.* This document can be found at the TI web site (www.ti.com) by searching on the key word PowerPAD. The document can also be ordered through your local TI sales office. Refer to literature number SLMA002 when ordering.

EVALUATION BOARD

An evaluation board is available for the THS6184. This board has been configured for proper thermal management of the THS6184. The circuitry has been designed for a typical ADSL application as shown previously in this document. To order the evaluation board contact your local TI sales office or distributor.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
THS6184PWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS6184PWPG4	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS6184PWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS6184PWPRG4	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS6184RHFR	ACTIVE	QFN	RHF	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS6184RHFRG4	ACTIVE	QFN	RHF	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS6184RHFT	ACTIVE	QFN	RHF	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS6184RHFTG4	ACTIVE	QFN	RHF	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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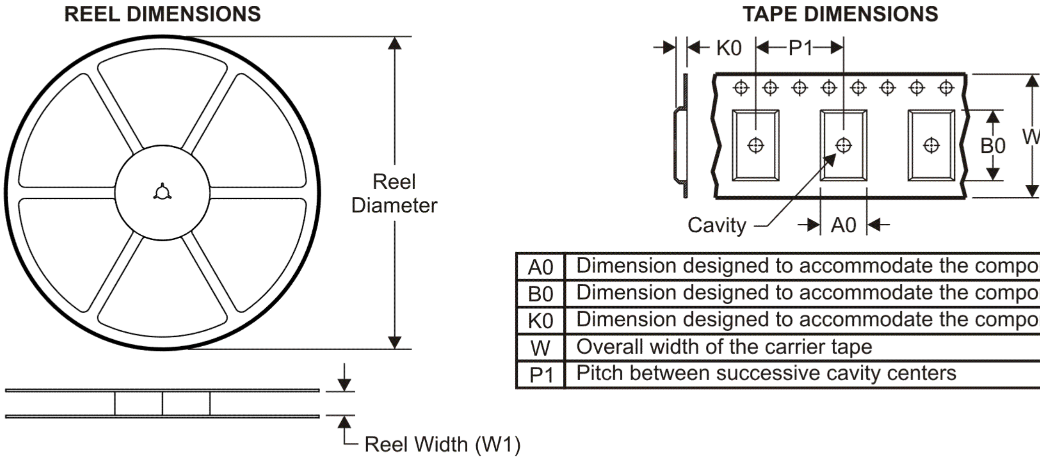
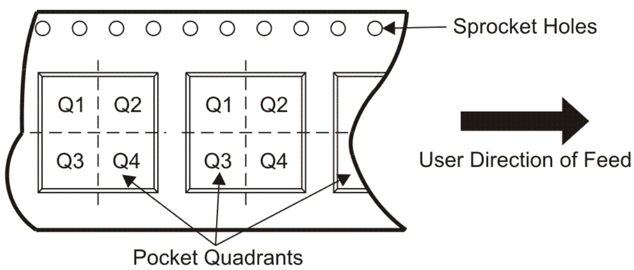
TAPE AND REEL INFORMATION



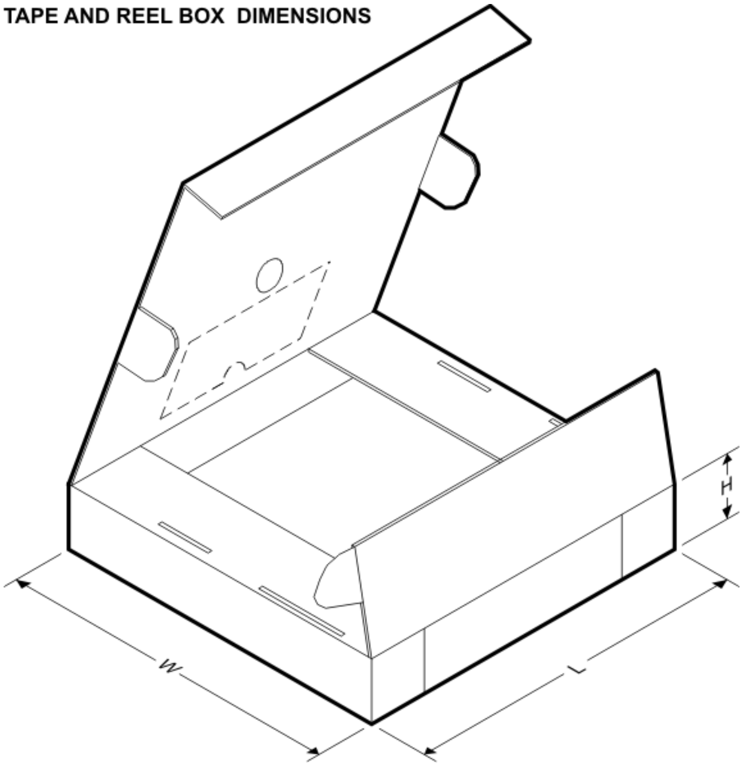
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS6184PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
THS6184RHFR	QFN	RHF	24	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
THS6184RHFT	QFN	RHF	24	250	180.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1

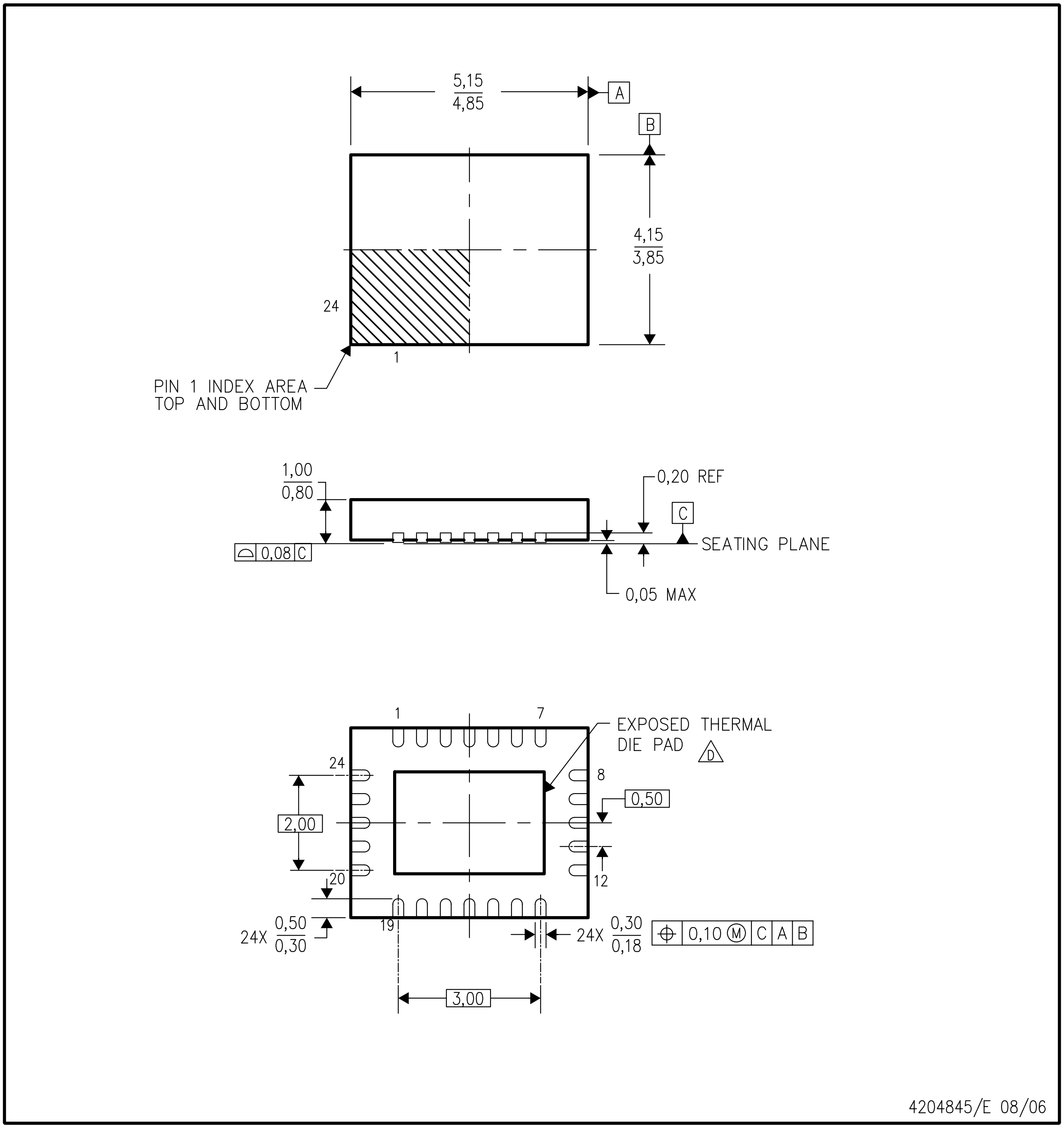
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS6184PWPR	HTSSOP	PWP	20	2000	346.0	346.0	33.0
THS6184RHFR	QFN	RHF	24	3000	346.0	346.0	29.0
THS6184RHFT	QFN	RHF	24	250	190.5	212.7	31.8

RHF (R-PQFP-N24) PLASTIC QUAD FLATPACK



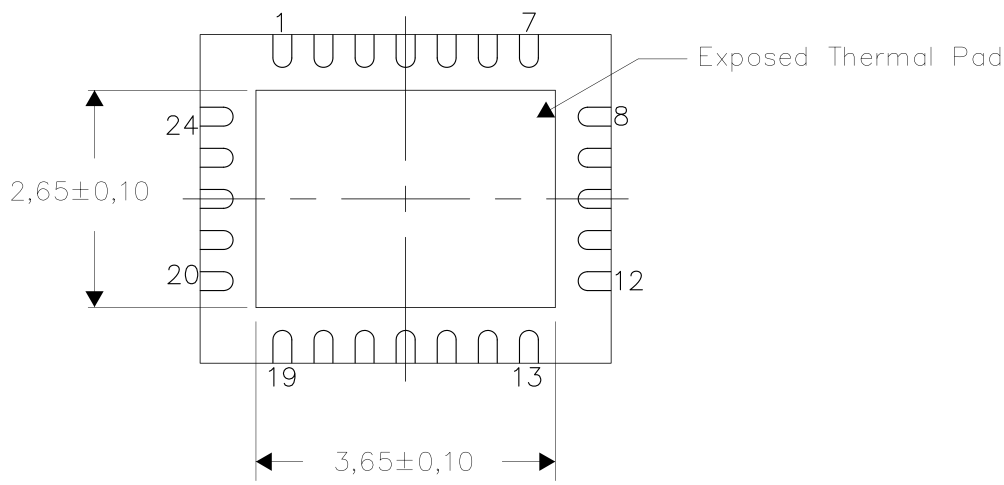
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No-Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO-220.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

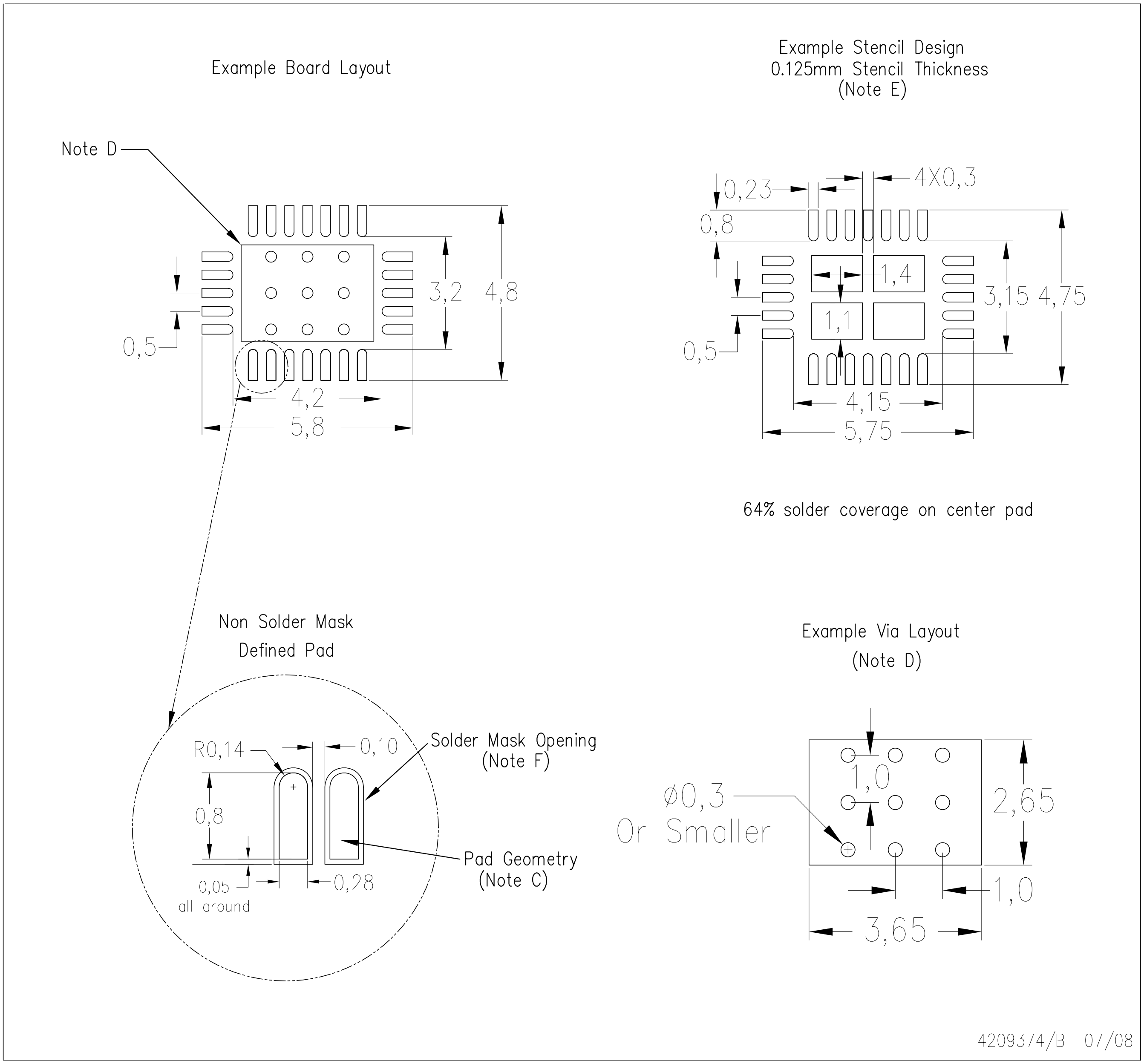


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

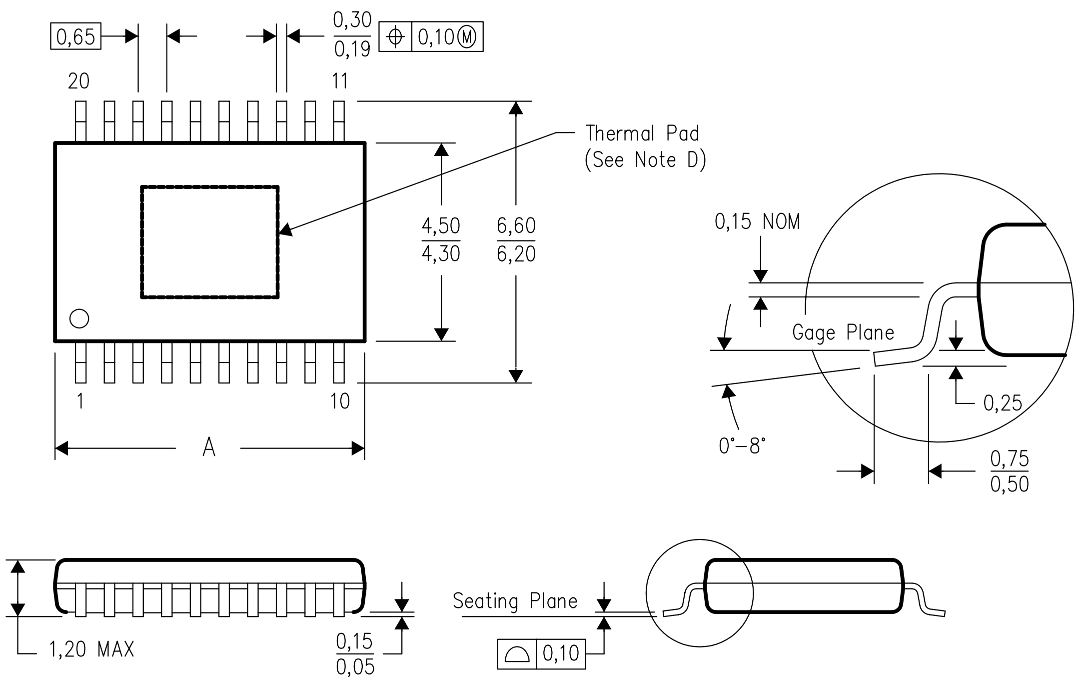
RHF (S-PVQFN-N24)



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

PWP (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE

20 PIN SHOWN



PINS ** / DIM	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/H 12/05

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
- E. Falls within JEDEC MO–153

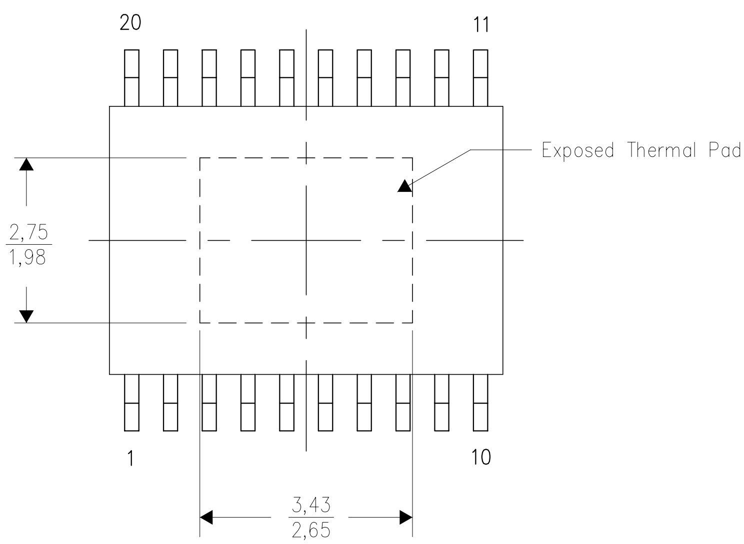
PowerPAD is a trademark of Texas Instruments.

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

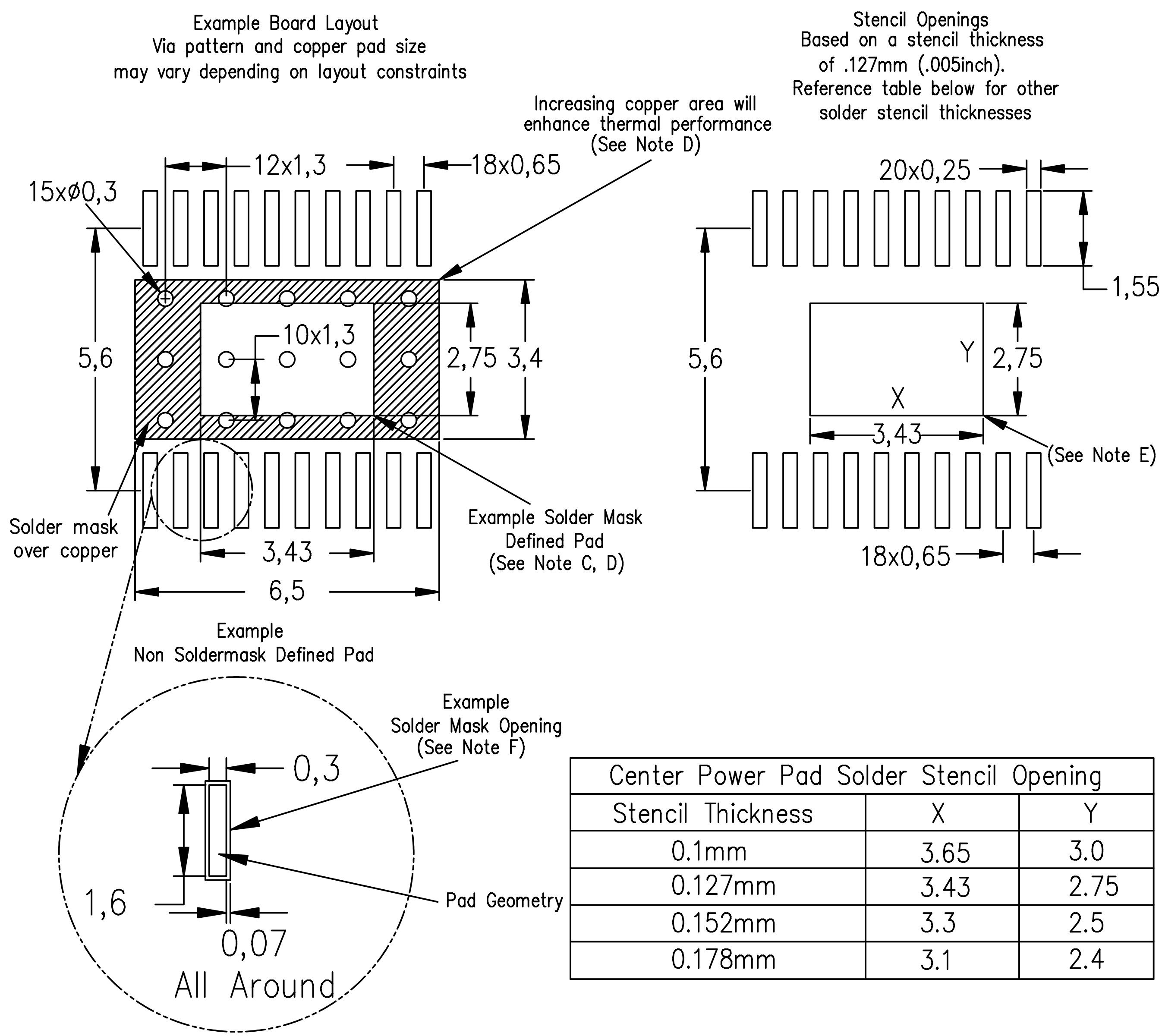


Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

PWP (R–PDSO–G20) PowerPAD™



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.65	3.0
0.127mm	3.43	2.75
0.152mm	3.3	2.5
0.178mm	3.1	2.4

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NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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